SYNOPSYS®

DesignWare® IP Family Reference Guide

June 2009

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Preface

About This Manual

This manual is a brief overview of the DesignWare Family of synthesizable and verification IP. For detailed product information, refer to individual product databooks and manuals mentioned in the following chapters.

Note

DesignWare Building Block component information has been moved from this document to a separate document, the *DesignWare Building Blocks Quick Reference Guide*.

Manual Overview

This manual contains the following chapters:

Preface	Describes the manual and typographical conventions and symbols; tells how to get technical assistance.
Chapter 1 "Overview"	Contains an overview and general description of the DesignWare Library product offering.
Chapter 1 "AMBA Bus Fabric and Peripheral IP"	Describes the available DesignWare Library AMBA/AXI Bus Fabric and Peripheral IP.
Chapter 2 "DesignWare Library Verification IP"	Describes the available DesignWare Library verification models.
Chapter 3 "DesignWare Foundry Libraries"	This chapter briefly describes the DesignWare Foundry Libraries.

Chapter 4 "DesignWare Cores (Digital and Mixed-Signal IP)"	Contains a brief description of each DesignWare Core.
Chapter 5 "DesignWare Star IP"	Contains a brief description of each DesignWare Star IP core.

Typographical and Symbol Conventions

Table 1 lists the conventions that are used throughout this document.

Table 1: Documentation Conventions

Convention	Description and Example
%	Represents the UNIX prompt.
Bold	User input (text entered by the user). `% cd $LMC_HOME/hdl`
`Monospace`	System-generated text (prompts, messages, files, reports). `No Mismatches: 66 Vectors processed: 66 Possible"`
Italic or *`Italic`*	Variables for which you supply a specific value. As a command line example: `% setenv LMC_HOME prod_dir` In body text: In the previous example, *prod_dir* is the directory where your product must be installed.
| (Vertical rule)	Choice among alternatives, as in the following syntax example: `-effort_level low | medium | high`
[ ] (Square brackets)	Enclose optional parameters: *`pin1`* `[`*`pin2 ... pinN`*`]` In this example, you must enter at least one pin name (*pin1*), but others are optional ([*pin2* … *pinN*]).
TopMenu > SubMenu	Pulldown menu paths, such as: **File > Save As …**

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You can find general Licensing (SCL) information on the Web at:

http://www.synopsys.com/Support/Licensing

Getting Help

If you have a question about using Synopsys products, please consult product documentation that is installed on your network or located at the root level of your Synopsys product CD-ROM (if available). You can also access documentation for DesignWare products on the Web:

- Product documentation for many DesignWare products:

  http://www.synopsys.com/dw/dwlibdocs.php

- Datasheets for individual DesignWare IP components, located using "Search for IP":

  http://www.synopsys.com/designware

You can also contact the Synopsys Support Center in the following ways:

- Open a call to your local support center by clicking this link and then accessing "Open a Support Case."

  http://www.synopsys.com/Support

- Support center contact information:

  http://www.synopsys.com/Support/GlobalSupportCenters

Comments?

To report errors or make suggestions, please send e-mail to:

support_center@synopsys.com.

To report an error that occurs on a specific page, select the entire page (including headers and footers), and copy to the buffer. Then paste the buffer to the body of your e-mail message. This will provide us with information to identify the source of the problem.

1 Overview

Synopsys DesignWare IP, the world's most widely-used, silicon-proven IP provides designers with a broad portfolio of synthesizable implementation IP, hardened PHYs and verification IP for ASIC, SoC and FPGA designs. The DesignWare family includes the following products:

- "DesignWare Library" on page 14 - contains the principal ingredients for design and verification including high speed datapath components, AMBA On-Chip Bus, memory portfolio, verification models of standard bus and I/Os, foundry libraries, popular Star IP cores and board verification IP.
- "VCS Verification Library" on page 20 - is a subset of the DesignWare Library and contains reusable, pre-verified verification IP of the industry's most popular bus and interface standards such as AMBA, PCI Express, PCI-X, PCI, USB On-the-Go, Ethernet, I^2C and thousands of memory models.
- "DesignWare Cores (Digital and Mixed-Signal)" on page 22 - silicon-proven, digital and mixed-signal standards-based connectivity IP such as PCI Express, PCI-X, PCI, USB 2.0 On-the-Go (OTG), USB 2.0 PHY, USB 1.1 and Ethernet.
- "DesignWare Star IP" on page 24 - high-performance, high-value cores from leading Star IP providers such as IBM, Infineon Technologies, MIPS Technologies, NEC and Philips.

DesignWare Library

The DesignWare Library provides designers with a comprehensive collection of synthesizable IP, verification IP and foundry libraries. The library contains the following principal ingredients for ASIC, SoC, and FPGA design and verification:

- Building Block IP (Datapath, Data Integrity, DSP, Test, and more)
- AMBA Bus Fabric, Peripherals, and Verification IP
- Memory portfolio (memory controller, memory BIST, memory models and more)
- Verification models of popular bus and I/O Standards (PCI Express, PCI-X, PCI, USB On-the-Go, and more)
- Microprocessor and DSP cores from industry-leading Star IP providers
- Foundry Libraries
- Board verification IP
- Microcontrollers (8051 and 6811)

A single license gives you access to all the IP in the library. For more information on the DesignWare Library, refer to the following:

http://www.synopsys.com/products/designware/dwlibrary.html

For a detailed search of the available IP, refer to the following:

http://www.synopsys.com/products/designware

Building Block IP

The DesignWare Building Block IP is a collection of over 200 technology-independent, high-quality, high-performance IP. Most of these IP elements include multiple implementations to provide a variety of performance and area tradeoff options.

Component groups for the Building Block IP are identified in the following table. For more detail, refer to the *DesignWare Building Blocks Quick Reference Guide*.

Component Group	Description	Component Type
Low Power	New components, and enhanced DWBB components that incorporate power-saving features, such as clock gating, piplining, and operand isolation. NOTE: A special implementation and license (“lpwr” / DesignWare-LowPower) is required to enable these new low power components and DWBB low power enhancements.	Synthesizable RTL
Datapath	Arithmetic, floating point, trigonometric, and sequential math IP	Synthesizable RTL
Data Integrity	Data integrity IP such as CRC, ECC, 8b10b...	Synthesizable RTL
Digital Signal Processing (DSP)	FIR and IIR filters	Synthesizable RTL
Application Specific	Debugger IP	Synthesizable RTL
Logic	Combinational, sequential, and control IP	Synthesizable RTL
Interface	Clock Domain Crossing (CDC)	Synthesizable RTL
Memory	Registers, FIFO, synchronous and asynchronous RAM, and stack IP	Synthesizable RTL
Test	JTAG IP such as boundary scan, TAP controller	Synthesizable RTL
GTECH	Technology-independent IP library to aid users in developing technology-independent parts	Synthesizable RTL

DesignWare AMBA Family of Components

AMBA is a standard bus architecture system developed by ARM for rapid development of processor-driven systems. The AMBA standard also allows a number of bus peripherals and resources to be connected in a consistent way. The following is a complete listing of the Synopsys DesignWare IP for the AMBA protocol.

Component Name	DesignWare AMBA Synthesizable IP
DW_ahb	AHB bus, arbitration, decode, and control logic (page 27)
DW_ahb_dmac	AHB Central Direct Memory Access (DMA) Controller (page 29)
DW_ahb_h2h	AHB to AHB Bridge (page 32)
DW_ahb_eh2h	Enhanced AHB to AHB Bridge (page 30)
DW_ahb_icm	AHB Multi-layer Interconnection Matrix (page 34)
DW_ahb_ictl	AHB Interrupt Controller (page 35)
DW_apb	APB bus, decode, and bridge (page 36)
DW_apb_gpio	APB General Purpose I/O (GPIO) (page 37)
DW_apb_i2c	APB I^2C Interface (page 38)
DW_apb_i2s	APB I^2S Interface (page 40)
DW_apb_ictl	APB Interrupt Controller (page 41)
DW_apb_rap	APB Remap & Pause (page 42)
DW_apb_rtc	APB Real Time Clock (page 43)
DW_apb_ssi	APB Synchronous Serial Interface (page 44)
DW_apb_timers	APB Timer (page 46)
DW_apb_uart	APB UART (page 47)
DW_apb_wdt	APB Watch Dog Timer (page 49)
DW_memctl	Memory Controller (page 65)
DW_axi	Multiple Address, Multiple Data AXI Interconnect (page 50)
DW_axi_gm	Generic Interface (GIF) to AMBA AXI Module (page 52)
DW_axi_gs	AMBA AXI Slave to Generic Interface (page 53)
DW_axi_hmx	Connects AMBA AXI Slave to AHB Master (page 54)

Component Name	DesignWare AMBA Synthesizable IP
DW_axi_rs	AMBA AXI Register Slice (page 55)
DW_axi_x2h	AXI to AHB Bridge (page 56)
DW_axi_x2p	AXI to APB Bridge (page 57)
DW_axi_x2x	AXI to AXI Bridge (page 59)
Component Name	**DesignWare AMBA Component Description — Verification IP**
ahb_bus_vmt ahb_master_vmt ahb_monitor_vmt ahb_slave_vmt	AHB Bus Interconnect (page 76) AHB Master (page 76) AHB Monitor (page 76) AHB Slave (page 76)
apb_master_vmt apb_monitor_vmt apb_slave_vmt	APB Master (page 78) APB Monitor (page 78) APB Slave (page 78)
axi_master_vmt axi_slave_vmt axi_monitor_vmt axi_interconnect_vmt	DesignWare VIP for AMBA 3 AXI (page 79)

DesignWare AMBA QuickStart

The DesignWare AMBA QuickStart (page 61) is a collection of example designs for AMBA subsystems built with DesignWare AMBA components. The QuickStart example designs are static, non-reconfigurable examples of complete subsystems that use DesignWare AMBA synthesizable IP and VIP components.

Star IP Microprocessor and DSP Cores

Component Name	Component Description	Component Type
DW_IBM460-S, DW_IBM405-S	PowerPC 440 32-Bit Microprocessor Cores from IBM (page 177)	Synthesizable RTL[a] Verification Model
DW_CoolFlux	CoolFlux 24-bit DSP Core from Philips (page 179)	Synthesizable RTL[a] Verification Model
DWC_n2p	Nios II Processor Core (page 182)	Synthesizable RTL[a]

a. Verification models of these cores are included in the DesignWare Library and the DesignWare Verification Library. Synthesizable RTL of these cores are available through the Star IP Program. For more information visit: http://www.synopsys.com/designware/star_ip.html.

Microcontrollers

Component Name	Component Description	Component Type
DW_6811	8-Bit Microcontroller (page 70)	Synthesizable RTL
DW8051	8-Bit Microcontroller (page 72)	Synthesizable RTL

Memory IP

Component Name	Component Description	Component Type
Memory Models	DesignWare contains thousands of pre-verified memory models, with over 10,000 devices from more than 25 vendors. (page 85)	Verification Models
DW_memctl	DesignWare Memory Controller (page 65)	Synthesizable RTL
DW_rambist	DesignWare Memory BIST solution (page 67)	Synthesizable RTL
DW Memory Building Block IP	DesignWare Building Block IP contains many memory-related IP. For details, see the *DesignWare Building Blocks Quick Reference Guide*	Synthesizable RTL

To view the complete DesignWare memory portfolio, refer to the following:

http://www.synopsys.com/memorycentral

Foundry Libraries

Synopsys is teaming with foundry leaders to provide DesignWare Library licensees access to standard cells and I/Os optimized for their process technologies. Each library includes a complete set of front-end and back-end views for Standard Cells and I/Os. Memory compilers are also included when available.

The current offering includes:

- TSMC Libraries for 0.15um, 0.13um and 90nm and 65nm, described on page 100.
- Chartered Libraries for 0.35um, 0.25um, 0.18um, and 0.13um, described on page 106.

Verification IP for Bus and I/O Standards

Component Name	Component Description	Type
ahb_bus_vmt, ahb_master_vmt, ahb_monitor_vmt, ahb_slave_vmt	DesignWare VIP for AMBA 2.0 AHB Models (page 76)	Verification
apb_master_vmt, apb_monitor_vmt, apb_slave_vmt	DesignWare VIP for AMBA 2.0 APB Models (page 78)	Verification
axi_master_vmt, axi_slave_vmt, axi_monitor_vmt, axi_interconnect_vmt	DesignWare VIP for AMBA 3 AXI (page 79)	Verification
ethernet_txrx_vmt, ethernet_monitor_vmt	10/100/1G/10G Ethernet Models (page 82)	Verification
enethub_fx, rmiirs_fx	Ethernet RMII Transceiver and Hub (page 83)	Verification
i2c_txrx_vmt	I^2C Bi-Directional Two-Wire Bus (page 84)	Verification
pcie_txrx_vmt, pcie_monitor_vmt	PCI Express 1.00a (page 88)	Verification
pcimaster_fx, pcislave_fx, pcimonitor_fx	PCI 2.3 and PCI-X 2.0 Simulation Models and Test Suite (page 90)	Verification
sata_device_vmt, sata_monitor_vmt	Serial ATA Models (page 92)	Verification
sio_txrx_vmt, sio_monitor_vmt	Serial Input/Output Interface Models (page 94)	Verification
usb_host_vmt, usb_device_vmt, usb_monitor_vmt	USB On-The-Go Models, 1.1, 2.0, OTG, UTMI, and UTMI+ Low Pin Interface (ULPI) (page 95)	Verification

Board Verification IP

The DesignWare Library contains over 18,500 simulation models for ASIC, SoC, and Board verification. For a complete search, visit http://www.synopsys.com/ipdirectory.

Component Group	Component Reference
VMT Models	Refer to "DesignWare Library Verification IP" on page 74
FlexModels	Refer to "DesignWare FlexModels" on page 96
DesignWare Memory Models	Refer to "Memory Models" on page 85
SmartModel Library	Refer to "DesignWare SmartModels" on page 98

VCS Verification Library

The VCS Verification Library contains a broad portfolio of verification IP for the industry's most popular bus protocols including AMBA 3 AXI, AMBA 2.0, PCI Express, USB 2.0 OTG, Ethernet, Serial ATA and thousands of memory models. The following table identifies the various components that make up this library.

Component Name	Component Description	Component Type
DesignWare Bus & I/O Standards		
ahb_bus_vmt, ahb_master_vmt, ahb_monitor_vmt, ahb_slave_vmt	DesignWare VIP for AMBA 2.0 AHB Models: AHB Bus Interconnect, AHB Master, AHB Monitor and AHB Slave (page 76)	Verification Models
apb_master_vmt, apb_monitor_vmt, apb_slave_vmt	DesignWare VIP for AMBA 2.0 APB Models: APB Master, APB Monitor and APB Slave (page 78)	Verification Models
axi_master_vmt axi_slave_vmt axi_monitor_vmt axi_interconnect_vmt	DesignWare VIP for AMBA 3 AXI (page 79)	Verification Model
ethernet_txrx_vmt, ethernet_monitor_vmt	10/100/1G/10G Gigabit Ethernet Models (page 82)	Verification Models
enethub_fx, rmiirs_fx	Ethernet RMII Transceiver and Hub (page 83)	Verification Models
i2c_txrx_vmt	I^2C Bi-Directional Two-Wire Bus (page 84)	Verification Model

pcie_txrx_vmt, pcie_monitor_vmt	PCI Express 1.00a (page 88)	Verification Model
pcimaster_fx, pcislave_fx, pcimonitor_fx	PCI/PCI-X Simulation Model and Test Suite (page 90)	Verification Models
usb_host_vmt, usb_device_vmt, usb_monitor_vmt	USB On-The-Go Models, 1.1, 2.0, OTG, UTMI, and UTMI+(page 95)	Verification Model
sio_txrxvmt, sio_monitor_vmt	Serial Input/Output Interface Models (page 94)	Verification Models
DesignWare Design Views of Star IP Cores		
DW_IBM460-S, DW_IBM405-S	PowerPC 440 Microprocessor Cores from IBM (page 177)	Verification Model
DW_CoolFlux	CoolFlux 24-bit DSP Core from Philips (page 179)	Verification Model
DWC_n2p	Nios II Processor Core (page 182)	Synthesizable RTL
DesignWare Memory		
Access to the full suite of memory IP is made available through DesignWare Memory Central; a memory-focused Web site that lets designers download DesignWare Memory IP and documentation. Visit Memory Central at: http://www.synopsys.com/products/designware/memorycentral		

Also visit the DesignWare Verification Library web page at:
http://www.synopsys.com/products/designware/dwverificationlibrary.html

DesignWare Cores (Digital and Mixed-Signal)

The DesignWare Cores shown in the following table provide system designers with silicon-proven, digital and analog connectivity IP. DesignWare Cores are licensed individually, on a fee-per-project business model.

Component Name	Component Description	Component Type
Ethernet Cores		
dwc_ethernet_mac10_100_universal	Ethernet MAC 10/100 Universal (page 111)	Synthesizable RTL
dwc_ether_mac10_100_1000_universal	Ethernet MAC 10/100/1G Universal (page 113)	Synthesizable RTL
Mobile Storage Core		
dwc_mobile_storage	Secure Digital (SD), Multimedia Card (MMC) and CE-ATA (page 119)	Synthesizable RTL
IEEE 1394 Cores		
dwc_1394_av_link	IEEE 1394 AVLink (page 121)	Synthesizable RTL
dwc_1394_cphy-native	IEEE 1394 Cable PHY (page 123)	Synthesizable RTL
JPEG Core		
dwc_jpeg	JPEG CODEC (page 129)	Synthesizable RTL
PCI Cores		
dwc_pci	32/64 bit, 33/66-MHz PCI Core (page 131)	Synthesizable RTL
dwc_pci-x	32/64 bit, 133-MHz PCI-X Core (page 133)	Synthesizable RTL
PCI Express Cores		
dwc_pci_express_ep	PCI Express Endpoint Core (page 138)	Synthesizable RTL
dwc_pci_express_rc	PCI Express Root Port Core (page 140)	Synthesizable RTL
dwc_pci_express_sw	PCI Express Switch Port Core (page 142)	Synthesizable RTL
dwc_pci_express_dm	PCI Express Dual Mode Core (page 144)	Synthesizable RTL
dwcore_pcie_phy	PCI Express PHY Core (page 146)	Hard IP

SATA Cores		
dwc_sata_ahci	SATA Host (page 148)	Synthesizable RTL
DWC_dsata	SATA Host (page 150)	Synthesizable RTL
dwc_sata_phy	SATA PHY (page 152)	Hard IP
USB Cores		
dwc_usb_1_1_device	USB 1.1. Device Controller (page 154)	Synthesizable RTL
dwc_usb_1_1_ohci_host	USB 1.1 OHCI Host Controller (page 156)	Synthesizable RTL
dwc_usb_1_1_hub-native	USB 1.1. Hub Controller (page 158)	Synthesizable RTL
dwc_usb_2_0_host_subsystem-pci-ahb	USB 2.0 Host Controller - UHOST2 (page 160)	Synthesizable RTL
dwc_usb_2_0_hs_otg_subsystem-ahb	USB 2.0 Hi-Speed On-the-Go Controller Subsystem (page 162)	Synthesizable RTL
dwc_usb_2_0_device	USB 2.0 Device Controller (page 164)	Synthesizable RTL
dwc_usb2_phy	USB 2.0 PHY (page 166)	Hard IP
dwc_usb2_hsotg_phy	USB 2.0 Hi-Speed On-the-Go PHY (page 168)	Hard IP
dwc_wiusb_device_controller	Wireless USB Device Controller (page 170)	Synthesizable RTL
dwc_usb2_nanophy	USB 2.0 nanoPHY (page 172)	Hard IP
XAUI		
dwc_xaui_phy	XAUI PHY (page 174)	Hard IP

Also visit the DesignWare Cores web page at:
http://www.synopsys.com/products/designware/dwcores.html

DesignWare Star IP

Synopsys offers DesignWare Library users the ability to evaluate and design easily at their desktop using the following high-performance, high-value IP cores from leading Star IP providers.

Component Name	Component Description	Component Type
DW_IBM460-S, DW_IBM405-S	PowerPC 440 Microprocessor Core from IBM (page 177)	Synthesizable RTL[a] Simulation Model
DW_CoolFlux	CoolFlux 24-bit DSP Core from NXP (page 179)	Synthesizable RTL[a] Simulation Model
DWC_n2p	Nios II Processor Core (page 182)	Synthesizable RTL[a] Simulation Model

a. Simulation models of these cores are included in the DesignWare Library and DesignWare Verification Library. Synthesizable RTL of these cores are available through the Star IP Program.

Also visit the DesignWare Star IP web page at:
http://www.synopsys.com/products/designware/star_ip.html

1 AMBA Bus Fabric and Peripheral IP

AMBA is a standard bus architecture system developed by ARM for rapid development of processor-driven systems. AMBA also allows a number of bus peripherals and resources to be connected in a consistent way. The following Synopsys DesignWare AMBA 2.0 and 3.0-compliant components are briefly described in this section:

Component Name	DesignWare AMBA Synthesizable IP
DW_ahb	AHB bus, arbitration, decode, and control logic (page 27)
DW_ahb_dmac	AHB Central Direct Memory Access (DMA) Controller (page 29)
DW_ahb_eh2h	Enhanced AHB to AHB Bridge (page 30)
DW_ahb_h2h	AHB to AHB Bridge (page 32)
DW_ahb_icm	AHB Multi-layer Interconnection Matrix (page 34)
DW_ahb_ictl	AHB Interrupt Controller (page 35)
DW_apb	APB bus, decode, and bridge (page 36)
DW_apb_gpio	APB General Purpose I/O (GPIO) (page 37)
DW_apb_i2c	APB I^2C Interface (page 38)
DW_apb_i2s	APB I^2S Interface (page 40)
DW_apb_ictl	APB Interrupt Controller (page 41)
DW_apb_rap	APB Remap & Pause (page 42)
DW_apb_rtc	APB Real Time Clock (page 43)
DW_apb_ssi	APB Synchronous Serial Interface (page 44)
DW_apb_timers	APB Timer (page 46)

Component Name	DesignWare AMBA Synthesizable IP
DW_apb_uart	APB UART (page 47)
DW_apb_wdt	APB Watch Dog Timer (page 49)
DW_memctl	Memory Controller (page 65)
DW_axi	Multiple Address, Multiple Data AXI Interconnect (page 50)
DW_axi_gm	Generic Interface (GIF) to AMBA AXI Module (page 52)
DW_axi_gs	AMBA AXI Slave to Generic Interface (page 53)
DW_axi_hmx	AMBA AXI Slave to AHB Master Interface (page 54)
DW_axi_rs	AMBA AXI Register Slice (page 55)
DW_axi_x2h	AXI to AHB Bridge (page 56)
DW_axi_x2p	AXI to APB Bridge (page 57)
DW_axi_x2x	AXI Master to AXI Slave Bridge (page 59)

A brief introduction to DesignWare AMBA components is available at the following location:

http://www.synopsys.com/products/designware/dw_amba.html

Source Licenses Available

You can configure any of the DesignWare AMBA synthesizable components and write out encrypted RTL using only a DesignWare license. If you want to write unencrypted RTL source code, you must purchase a special source license. For more information about licenses, please refer to the *DesignWare AMBA Synthesizable Components Installation Guide*:

www.synopsys.com/products/designware/docs/doc/amba/latest/dw_amba_install.pdf

DesignWare AMBA QuickStart

The DesignWare AMBA QuickStart (page 61) is a collection of example designs for AMBA subsystems built with DesignWare AMBA synthesizable components. The QuickStart example designs are static, non-reconfigurable examples of complete subsystems that use DesignWare AMBA synthesizable and verification components.

AMBA Compliant

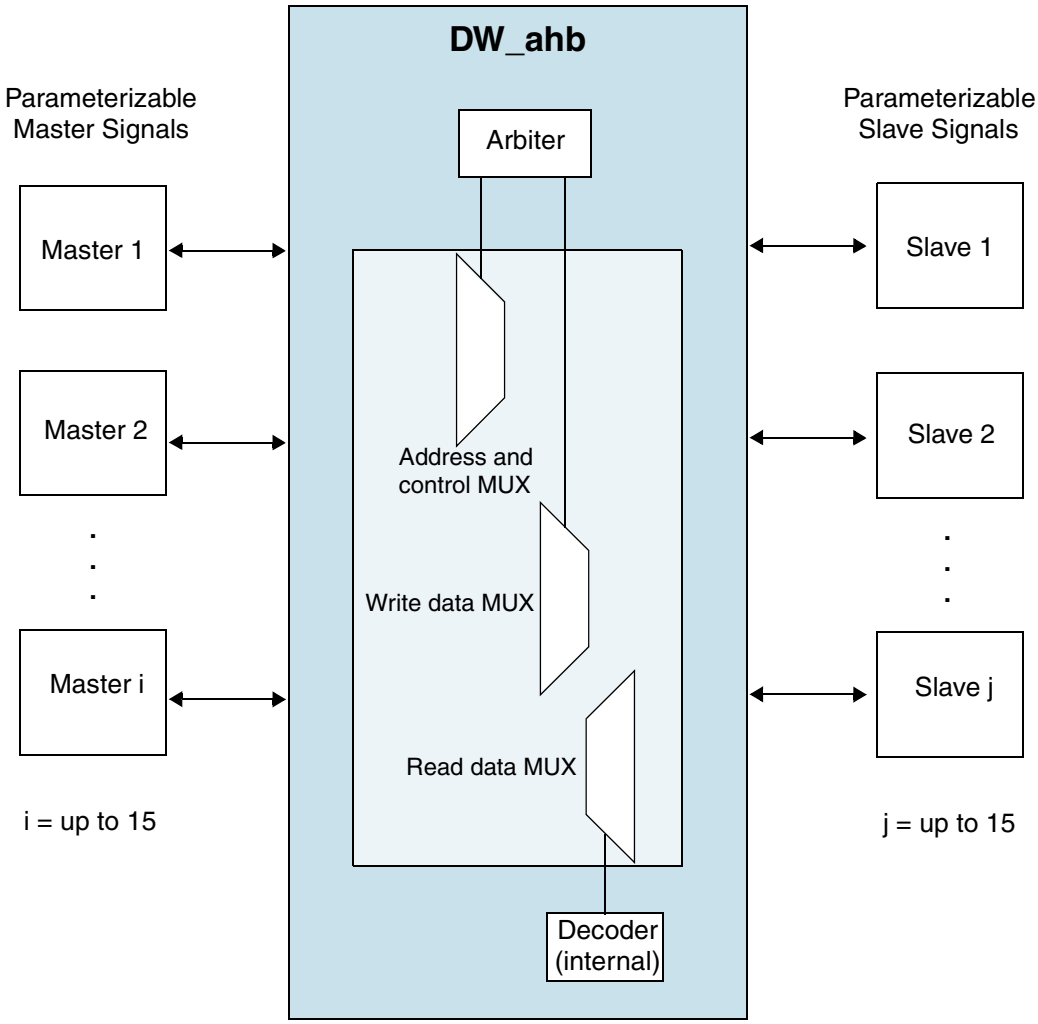
DW_ahb
Advanced High-Performance Bus

- Configuration of AMBA Lite system
- Configuration of up to 15 masters in a non-AMBA Lite system
- Configuration of up to 15 slaves
- Configuration of data bus width of up to 256 bits
- System address width of 32 or 64 bits
- Configuration of system endianness — big or little endian; can be controlled by external input or set during configuration of component
- Optional arbiter slave interface
- Optional internal decoder
- Programmable arbitration scheme:
- Weighted token
- Programmable or fixed priority
- Fair-Among-Equals
- Arbitration for up to 15 masters
- Individual grant signals for each master
- Support for split, burst, and locked transfers
- Optional support for early burst termination
- Configurable support for termination of undefined length bursts by masters of equal or higher priority
- Configurable or programmable priority assignments to masters
- Disabling of masters and protection against self disable
- Optional support for AMBA memory remap feature
- Optional support for pausing of the system, immediately or when bus is IDLE
- Contiguous and non-contiguous memory allocation options for slaves
- External debug mode signals, giving visibility

Also, see the block diagram on the following page.

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html



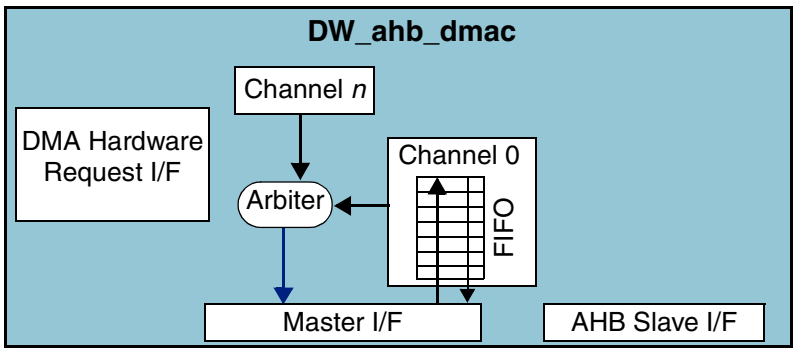
The *DesignWare DW_ahb Databook* is available at:

http://www.synopsys.com/products/designware/docs

DW_ahb_dmac

AHB Central Direct Memory Access (DMA) Controller

- AHB slave interface – used to program the DW_ahb_dmac
- AHB master interface(s)
  - Up to four independent AHB master interfaces that allows:
    - Up to four simultaneous DMA transfers
    - Masters that can be on different AMBA layers (multi-layer support)
    - Source and destination that can be on different AMBA layers (pseudo fly-by performance)
  - Configurable data bus width (up to 256 bits) for each AHB master interface
  - Configurable endianness for master interfaces
- Configurable identification register
- Encoded parameters
- Channels
  - Up to eight channels, one per source and destination pair
  - Unidirectional channels – data transfers in one direction only
  - Programmable channel priority
- Transfers
  - Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
  - DW_ahb_dmac to or from APB peripherals through the APB bridge
- Component parameters for configurable software driver support
- coreAssembler ready.



The *DesignWare DW_ahb_dmac Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_ahb_eh2h

Enhanced AHB to AHB Bridge

Clocks

- Asynchronous or synchronous clocks, any clock ratio
- Fully registered outputs
- Optional pipeline stages to reduce logic levels on bus inputs

AHB Slave interface

- Data width: 32,64,128, or 256 bits
- Address width: 32 or 64 bits
- Big or little endian
- Zero or two wait states OKAY response
- ERROR response
- No RETRY response
- SPLIT response
- HSPLIT generation
- Handling of multiple, outstanding split transactions
- Multiple HSELs
- HREADY low (alternative to SPLIT response) operation mode

Software interface

- Interrupt signal on write errors
- Interrupt status/clear registers

Sideband signals

- Input sstall pin to qualify an address phase for HREADY low operation mode
- Output sflush pin to monitor the flushing operation on the read buffer

AHB Master interface

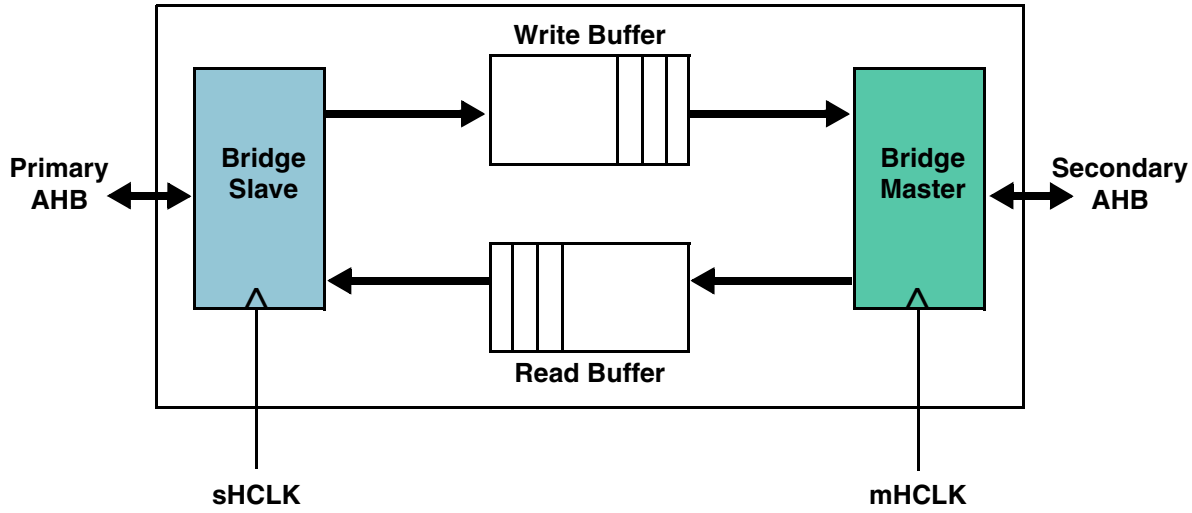
- Data width: 32,64,128, or 256 bits
- Address width: 32 or 64 bits
- Big or little endian
- Lock and bus request generation
- SINGLE, INCR burst type generation for writes
- Any burst type generation for reads
- Downsizing of wider transfers

Write operations

- Configurable depth write buffer
- Buffered writes (always, HPROT is don't care)
- SPLIT response on write buffer full
- Maximum of two wait states on non-sequential access
- Zero wait states (full bandwidth) on sequential access
- Zero BUSY cycles (full bandwidth), secondary burst generation

Read operations

- Configurable depth read buffer
- Pre-fetched reads
- Non-prefetched reads
- SPLIT response on non-sequential (non yet prefetched) access
- Zero wait states (full bandwidth) on prefetched read data



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_ahb_eh2h Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_ahb_h2h

AHB to AHB Bridge

System Level

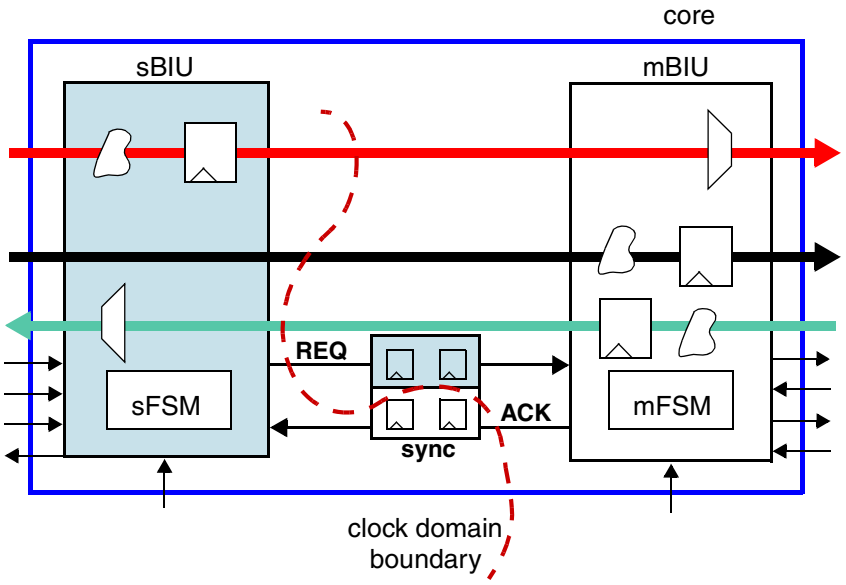
- Configurable asynchronous or synchronous clocks – any clock ratio
- Four clocking modes for synchronous clock configurations – two with and two without clock enables
- Low-gate count implementation (minimum configuration below 2K gates)
- Sub-optimal throughput performance (non-buffered architecture)
- High clock-speed operations (fully registered outputs, operating frequency more than 300 MHz)

AHB Master Interface

- Configurable AHB address width (32 or 64 bits)
- Configurable AHB data width (32, 64, 128, or 256 bits)
- Configurable endianness
- HLOCK generation
- HBUSREQ generation
- HTRANS: generation of IDLE or NSEQ bus cycles
- Non-pipelined transfers: address phase always followed by IDLE cycles until data phase completes
- HBURST: fixed to SINGLE
- All other AHB control signals forwarded unchanged
- AHB Lite configuration to remove redundant logic
- Deadlock detection

AHB Slave Interface

- Deadlock protection: SPLIT response generation after deadlock detection at the master interface
- Bus held off (HREADY low) until the secondary transfer data phase completes and is acknowledged back from the master interface
- SPLIT response (from secondary) forwarded back to primary as RETRY
- Component ID code retrievable from read data bus
- Support for locked transfers (any HTRANS) through HMASTLOCK
- IDLE and BUSY non-locked cycles ignored



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_ahb_h2h Databook* is available at:

http://www.synopsys.com/products/designware/docs

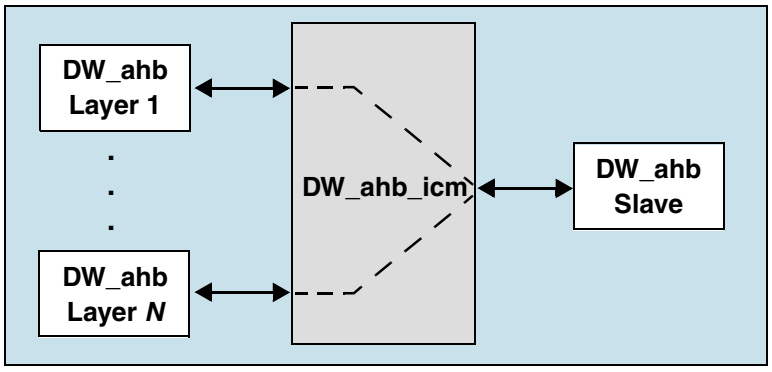
AMBA Compliant

DW_ahb_icm

AHB Multi-layer Interconnection Matrix

- Layer arbitration and master multiplexing
- Input stage address and control holding registers for each layer
- Mapping of slave response onto correct layer
- Returning of splits onto the correct layer
- Common clock and reset shared amongst all layers
- coreAssembler ready.

- User-defined parameters:
  - AMBA Lite
  - AHB address bus width, (same width on all layers)
  - AHB data bus width, (same width on each layer)
  - AHB master layers, (up to 4)
  - Split or non-split capable slave
  - Slave with/without multiple select lines
  - Slave with/without protection control
  - Slave with/without burst control
  - Slave with/without lock control
  - Layer release scheme
  - Baseline arbitration scheme
  - External arbitration priority control



The *DesignWare DW_ahb_icm Databook* is available at:

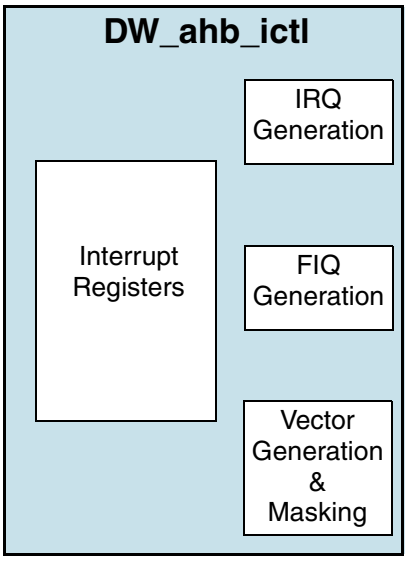
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_ahb_ictl

AHB Interrupt Controller

- 2 to 64 IRQ normal interrupt sources
- 1 to 8 FIQ fast interrupt sources (optional)
- Vectored interrupts (optional)
- Software interrupts
- Configuration ID registers
- Priority filtering (optional)
- Masking
- Scan mode (optional)
- Programmable interrupt priorities (after configuration)
- Encoded parameters
- Note: Does not support split transfers



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

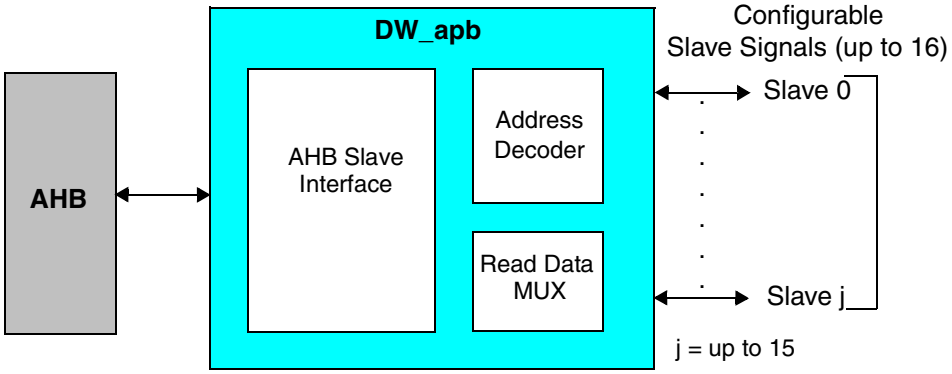
The *DesignWare DW_ahb_ictl Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb
Advanced Peripheral Bus

- APB Bridge and APB bus functionality incorporated
- AHB slave
- Supports up to 16 APB slaves
- Supports big- and little-endian AHB systems
- Supports little-endian APB slaves
- Supports 32, 64, 128, 256 AHB data buses
- Supports 8, 16, and 32-bit APB data buses
- Supports single and burst AHB transfers
- Supports synchronous hclk/pclk; hclk is an integer multiple of pclk
- The AHB slave side does not support SPLIT, RETRY or ERROR responses



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb Databook* is available at:

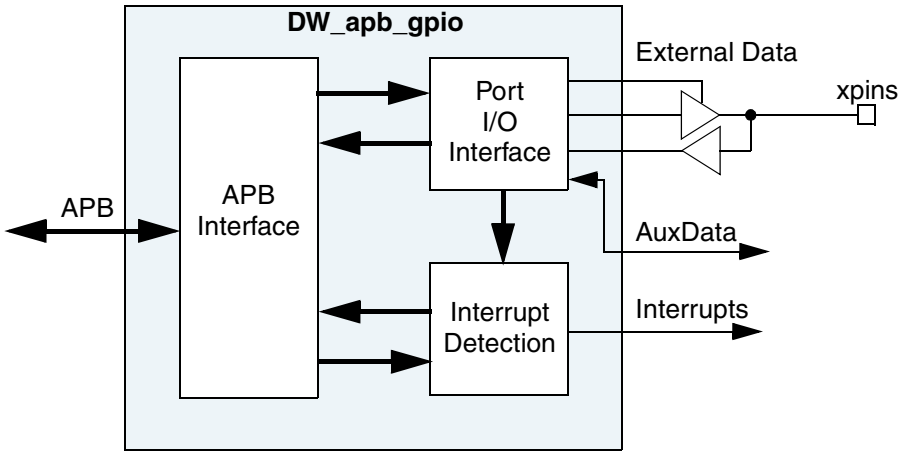
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_gpio

APB General Purpose Programmable I/O

- Up to 128 independently configurable pins (If more than 128 pins are required, another DW_apb_gpio should be instantiated.)
- Up to four ports, A to D, which are separately configurable
- Separate data registers and data direction registers for each port
- Configurable hardware and software control for each port, or for each bit of each port.
- Separate auxiliary data input, data output, and data control for each I/O in Hardware Control mode
- Independently controllable port bits
- Configurable interrupt mode for Port A
- Configurable debounce logic with an external slow clock to debounce interrupts
- Option to generate single or multiple interrupts
- GPIO Component Type register
- GPIO Component Version register
- Configurable reset values on output ports



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_gpio Databook* is available at:

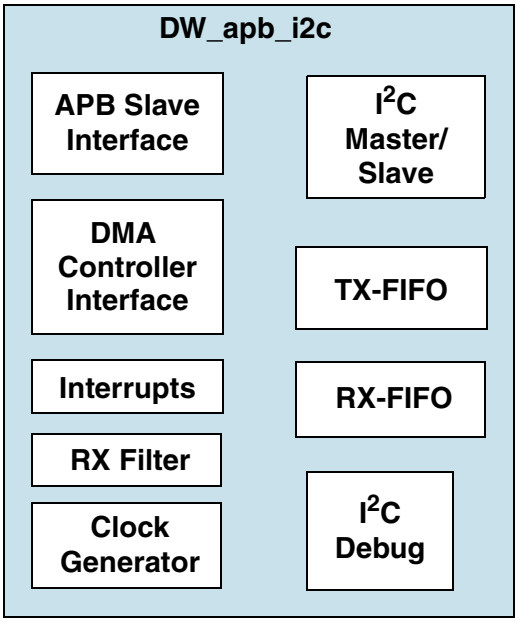
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_i2c

APB I2C Interface

- Two-wire I2C serial interface
- Three speeds:
  - Standard mode (100 Kb/s)
  - Fast mode (400 Kb/s)
  - High-speed mode (3.4 Mb/s)
- Supports clock synchronization
- Master or slave I2C operation
- Supports multi-Master operation (bus arbitration)
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Slave bulk transfer mode
- Component parameters for configurable software driver support
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus)
- Transmit and receive buffers
- Interrupt or polled mode operation
- Handles Bit and Byte waiting at all bus speeds
- Simple software interface consistent with DesignWare APB peripherals
- Digital filter for the received SDA and SCL lines
- Support for APB data bus widths of 8, 16, and 32 bits
- DMA handshaking interface compatible with the DW_ahb_dmac handshaking interface



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_i2c Databook* is available at:

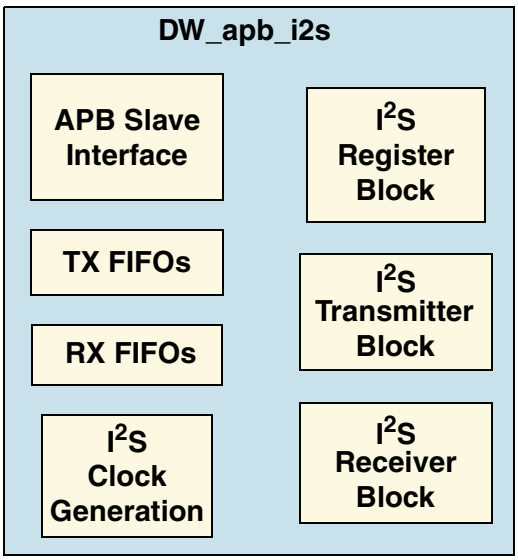
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_i2s

APB I2S Bus

- APB data bus widths of 8, 16, and 32 bits
- I2S transmitter and/or receiver based on the Philips I2S serial protocol
- Configurable number of stereo channels (up to 4) for both transmitter and receiver
- Full duplex communication due to the independence of transmitter and receiver
- Asynchronous clocking of APB bus and I2S sclk
- Master or slave mode of operation
- Audio data resolutions of 12, 16, 20, 24, and 32 bits
- External sclk gating and enable signals
- Configurable FIFO depth of 2, 4, 8, 16 bits
- Configurable support for programmable DMA registers
- Programmable FIFO thresholds
- Component parameters for configurable software driver support



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_i2s Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

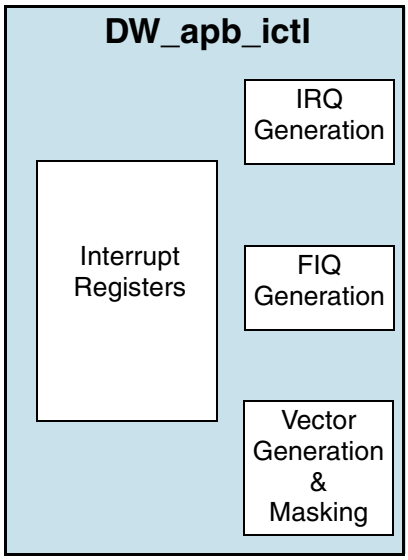
DW_apb_ictl

APB Interrupt Controller

- 2 to 64 IRQ normal interrupt sources
- 1 to 8 FIQ fast interrupt sources (optional)
- Vectored interrupts (optional)
- Software interrupts
- Priority filtering (optional)
- Masking
- Scan mode (optional)
- Programmable interrupt priorities (after configuration)

Note

DW_apb_ictl is an exact replacement for the original component DW_amba_ictl (name change only).



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

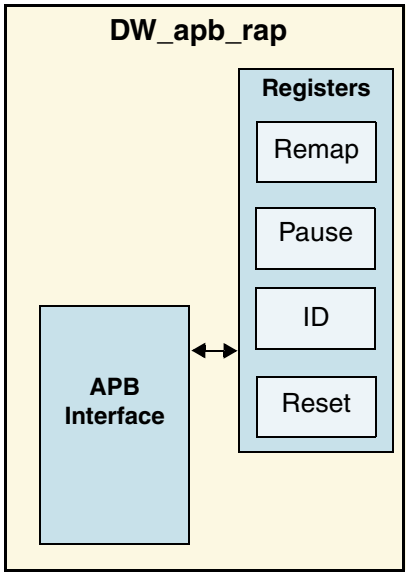
The *DesignWare DW_apb_ictl Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_rap
APB Remap and Pause

- Configuration of APB data bus width 8, 16, or 32
- Remap Control: Used to switch the DW_ahb address decoder from boot mode to normal mode operation.
- Pause Mode: Used to put the DW_ahb's arbiter into low-power (pause) mode.
- In pause mode the dummy master is granted the AHB bus until an interrupt occurs.
- Reset Status Register: Keeps track of status from up to eight separate system reset signals.
- Identification Code Register: Implements a configurable, read-only ID register



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_rap Databook* is available at:

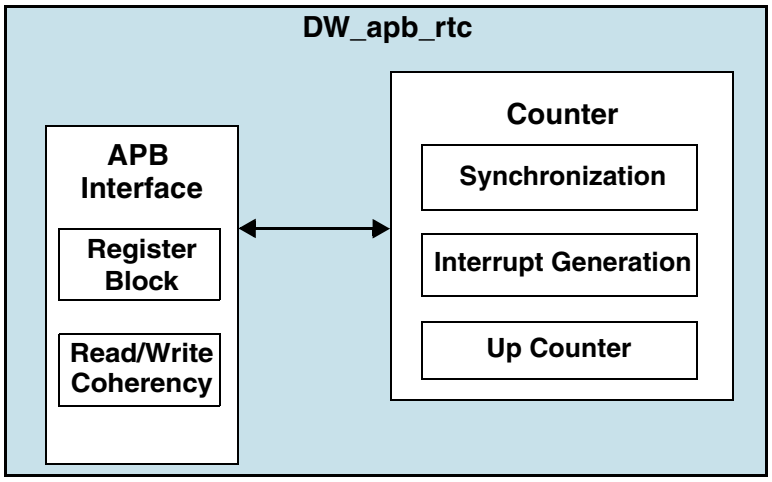
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_rtc

APB Real Time Clock

- APB slave interface with read/write coherency for registers
- Incrementing counter and comparator for interrupt generation
- Free-running pclk
- User-defined parameters:
  - APB data bus width
  - Counter width
  - Clock relationship between bus clock and counter clock
  - Interrupt polarity level
  - Interrupt clock domain location
  - Counter enable mode
  - Counter wrap mode
- Some uses of the DW_apb_rtc are:
  - Real-time clock – used with software for keeping track of time
  - Long-term, exact chronometer – When clocked with a 1 Hz clock, it can keep track of time from now up to 136 years in the future
  - Alarm function – generates an interrupt after a programmed number of cycles
  - Long-time, base counter – clocked with a very slow clock signal



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_rtc Databook* is available at:

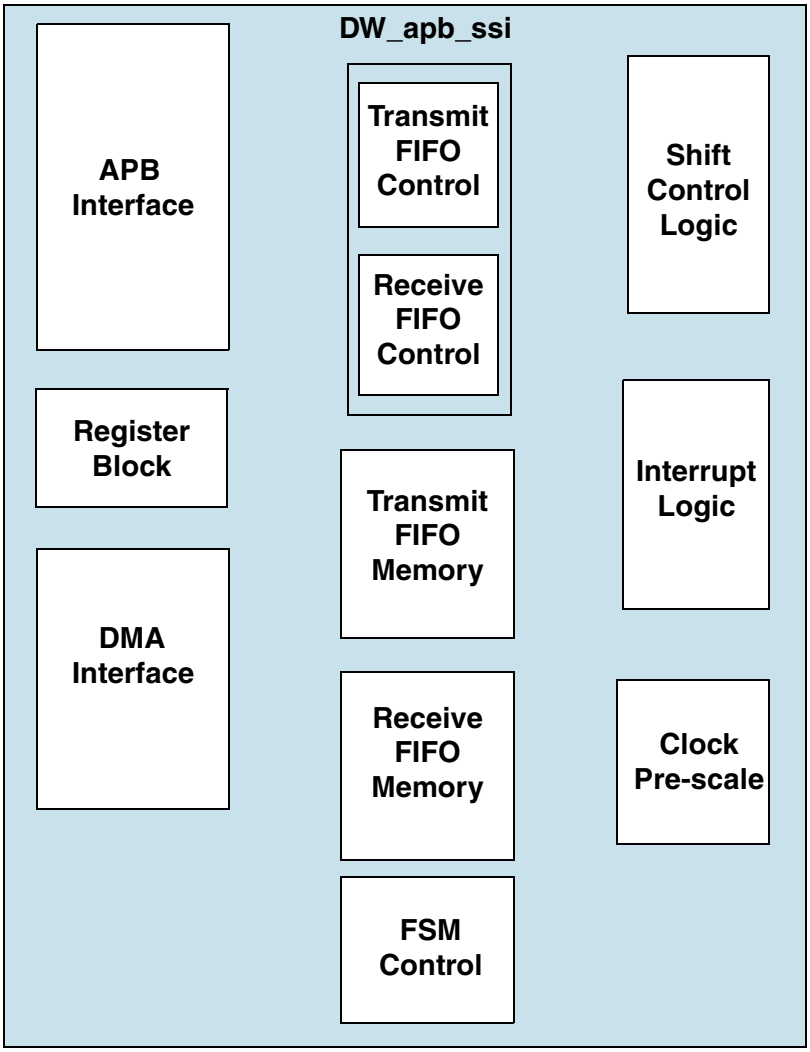
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_ssi

APB Synchronous Serial Interface

- AMBA APB interface – Allows for easy integration into an AMBA System on Chip (SoC) implementation.
- Scalable APB data bus width – Supports APB data bus widths of 8, 16, and 32 bits.
- Serial-master or serial-slave operation – Enables serial communication with serial-master or serial-slave peripheral devices.
- DMA Controller Interface – Enables the DW_apb_ssi to interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
- Independent masking of interrupts – Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Bypass of meta-stability flip-flops for synchronous clocks – When the APB clock (pclk) and the DW_apb_ssi serial clock (ssi_clk) are synchronous, meta-stable flip-flops are not used when transferring control signals across these clock domains.
- Programmable features:
  - Serial interface operation – Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
  - Clock bit-rate – Dynamic control of serial bit rate of data transfer; used in only serial-master mode.
  - Data Item size (4 to 16 bits) – Item size of each data transfer under control of programmer.
- Configurable features:
  - FIFO depth – Configurable depth of transmit and receive FIFO buffers from 2 to 256 words deep; FIFO width fixed at 16 bits.
  - Number of slave select outputs – When operating as serial master, 1 to 16 serial slave-select output signals can be generated.
  - Hardware/software slave-select – Dedicated hardware slave-select lines or software control for targeting serial-slave device.
  - Combined or individual interrupt lines
  - Interrupt polarity – Selects serial-clock phase of SPI format directly after reset.



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_ssi Databook* is available at:

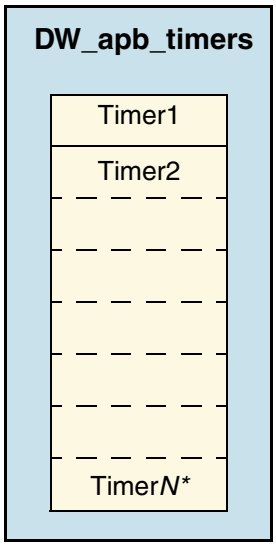
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_timers

APB Programmable Timers

- Up to eight programmable timers
- Configurable timer width: 8 to 32 bits
- Support for two operation modes: free-running and user-defined count
- Support for independent clocking of timers
- Configurable polarity for each individual interrupt
- Configurable option for a single or combined interrupt output flag
- Configurable option to have read/write coherency registers for each timer
- Configurable option to include timer toggle output, which toggles each time counter reloads



* *N* <= 8

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_timers Databook* is available at:

http://www.synopsys.com/products/designware/docs

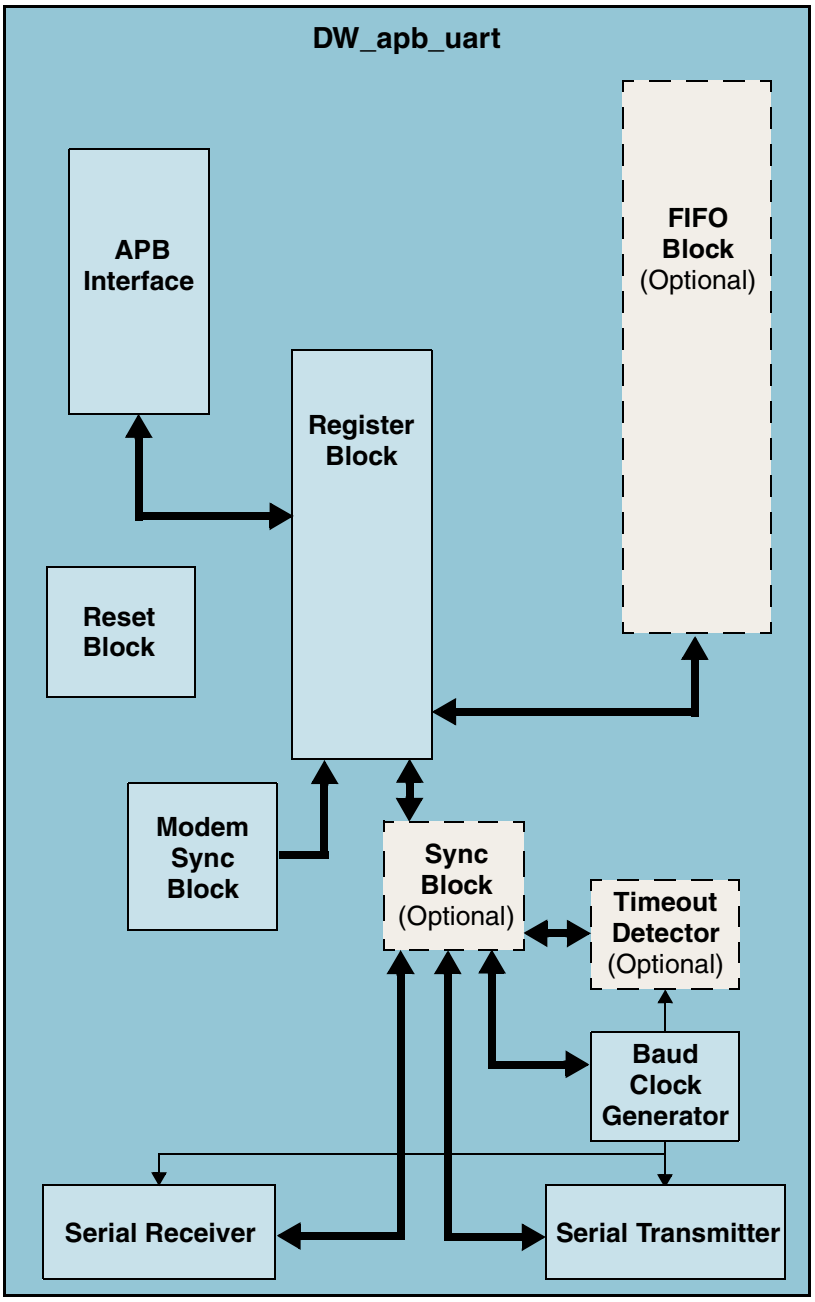
AMBA Compliant

DW_apb_uart

APB Universal Asynchronous Receiver/Transmitter

- AMBA APB interface allows easy integration into AMBA SoC implementations
- Configurable APB data bus widths of 8, 16 and 32
- Functionality based on the 16550 industry standard, that is as follows:
  - Programmable character properties, such as number of data bits per character (5-8), optional parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)
  - Line break generation and detection
  - DMA signaling with two programmable modes
  - Prioritized interrupt identification
- Configurable selection of additional DMA interface signals for compatibility with DesignWare DMA interface
- Configurable selection of DMA interface signal polarity
- Configurable transmit and receive FIFO depths of none, 16, 32, 64,…,2048
- Configurable internal or external FIFO (RAM) selection
- Programmable FIFO enable/ disableExternal read enable signal for RAM wake-up when using external RAMs
- Configurable selection of the use two clocks (pclk and sclk) instead of one (pclk)
- Programmable Auto Flow Control mode as specified in the 16750 standard
- Programmable Transmitter Holding Register Empty (THRE) interrupt mode
- Configurable IrDA 1.0 SIR mode support with up to 115.2 Kbaud data rate and a pulse duration (width) as follows: width = 3/16 × *bit period* as specified in the IrDA physical layer specification
- Programmable serial data baud rate
- Configurable baud clock reference output signal
- Modem and status lines are independently controlled
- Programmable Loopback mode that enables greater testing of Modem Control and Auto Flow Control features (Loopback support in IrDA SIR mode is available)
- Selectable clock gate enable output(s) used to indicate that the TX and RX pipeline is clear (no data) and no activity has occurred for more than one character time, so clocks may be gated
- Separate system resets for each clock domain to prevent metastability
- Selectable FIFO access mode (for FIFO testing) so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master

Also see the block diagram on the following page.



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_apb_uart Databook* is available at:

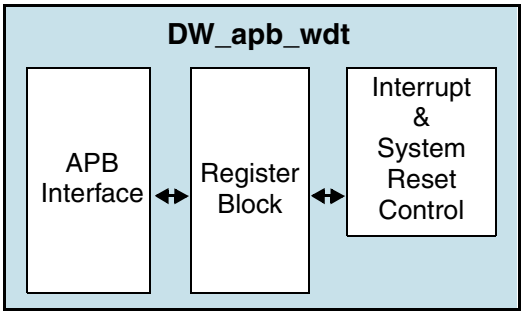
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_apb_wdt

APB Watchdog Timer

- AMBA APB interface used to allow easy integration into AMBA System-on-Chip (SoC) implementations.
- Configurable APB data bus widths of 8, 16, and 32 bits.
- Configurable watchdog counter width of 16 to 32 bits.
- Counter counts down from a pre-set value to zero to indicate the occurrence of a timeout.
- Optional external clock enable signal to control the rate at which the counter counts.
- If a timeout occurs the DW_apb_wdt can perform one of the following operations:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable timeout range (period). The option of hard coding this value during configuration is available to reduce the register requirements.
- Optional dual programmable timeout period, used when the duration waited for the first kick is different than that required for subsequent kicks. The option of hard coding these values is available.
- Programmable and hard coded reset pulse length.
- Prevention of accidental restart of the DW_apb_wdt counter.
- Prevention of accidental disabling of the DW_apb_wdt.
- Optional support for Pause mode with the use of external pause enable signal.
- Test mode signal to decrease the time required during functional test.
- coreAssembler ready.



The *DesignWare DW_apb_i2c Databook* is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_axi

Multiple Address, Multiple Data AXI Interconnect

- High performance multiple address bus, multiple data (MAMD) bus AXI interconnect architecture
- Configurable number of master and slave ports (up to 16 each)
- Configurable system decoder (optional)
- Configurable master and slave priorities used for arbitration (configured statically or driven dynamically through input ports)
- Default slave included
- Configurable slave visibility per master
- Built-in out-of-order deadlock avoidance
- Address width of 32 or 64 bits
- coreAssembler ready
- Data widths of 8, 16, 32, 64, 128, 256, and 512 bits
- Equal data widths of master and slave ports
- Support for data bursts up to 256 beats
- Single clock frequency for all master and slave ports
- Equal data widths of master and slave ports
- No buffering of AXI channel payload in interconnect
- Locked transfer support
- Automatically optimized in single AXI master subsystems
- Optional user sideband signals for each AXI channel, allowing additional control/status per channel (for example, data parity)

The following page contains a block diagram of the DW_axi.

Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs

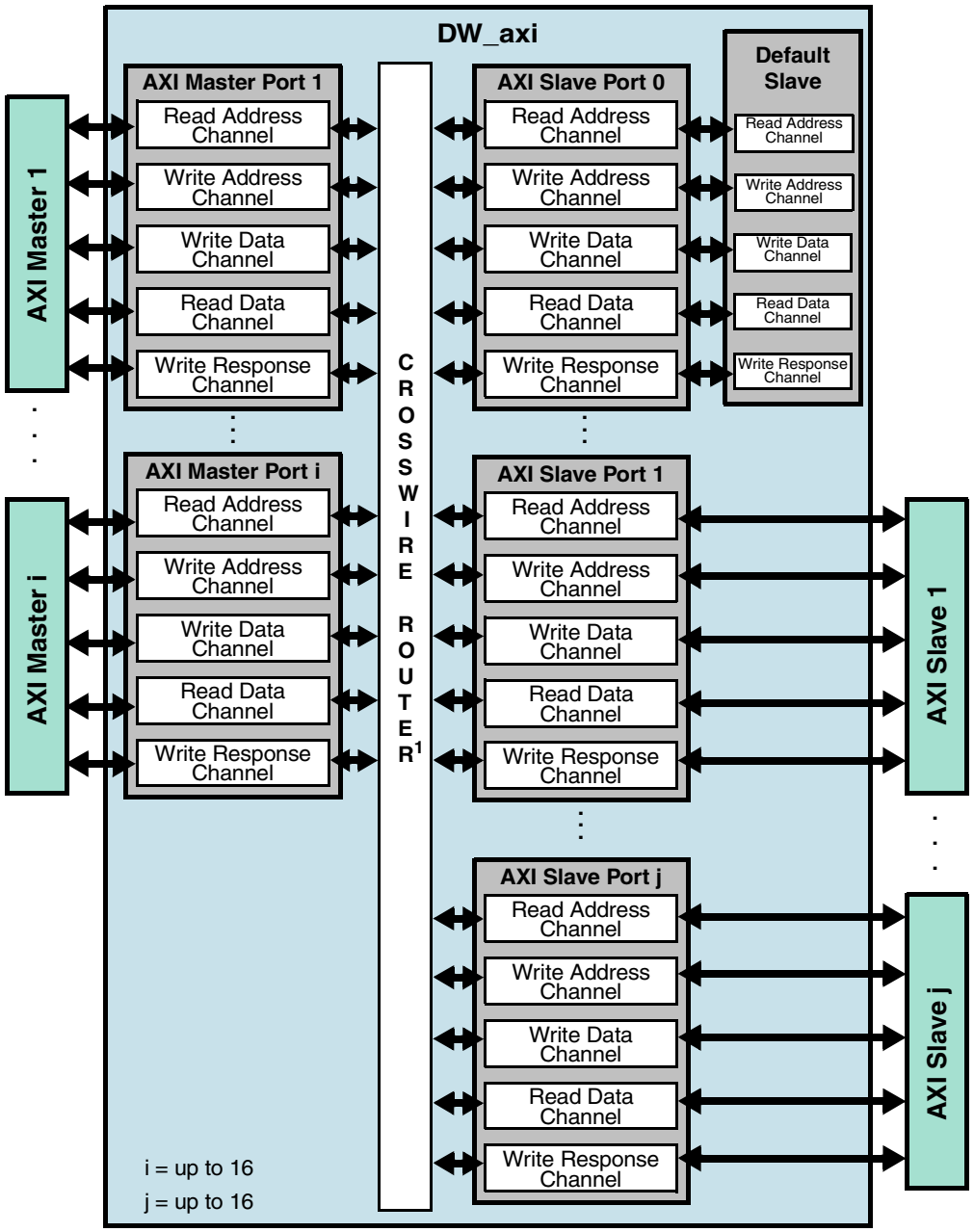
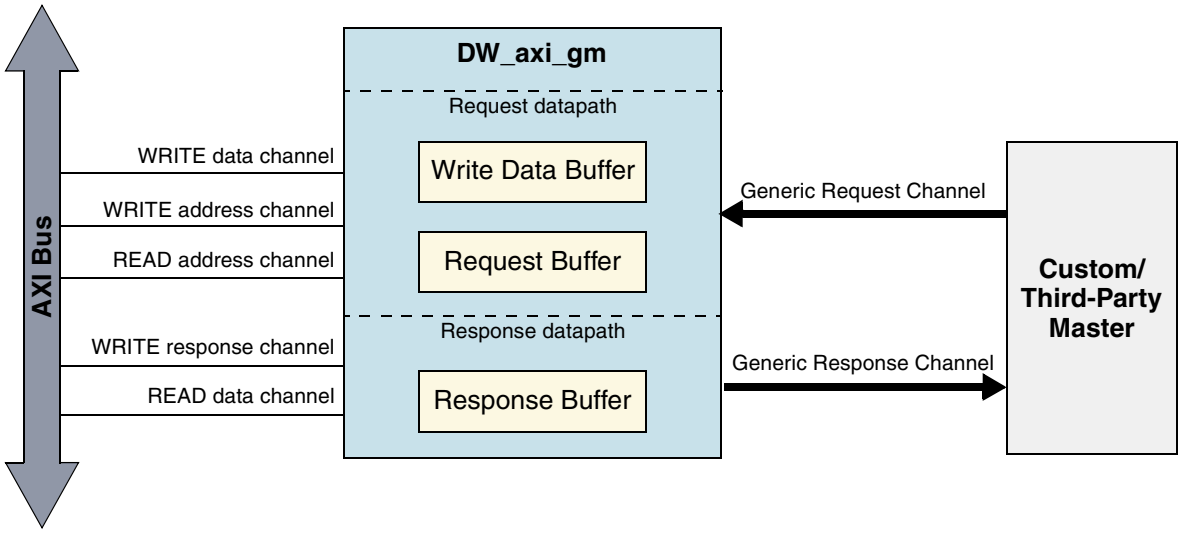


Figure 1: DW_axi Block Diagram

DW_axi_gm

Generic Interface (GIF) to AMBA AXI Module

- Full support of the AXI protocol, except for exclusive accesses
- Full support of AXI low-power interface
- Two-way flow control
- Synchronous point-to-point communication on generic interface (GIF)
- Independent request and response GIF channels
- Unlimited outstanding transactions
- Synchronous clock support; including slower GIF clock
- Configurable micro-architecture
- Transaction block control



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

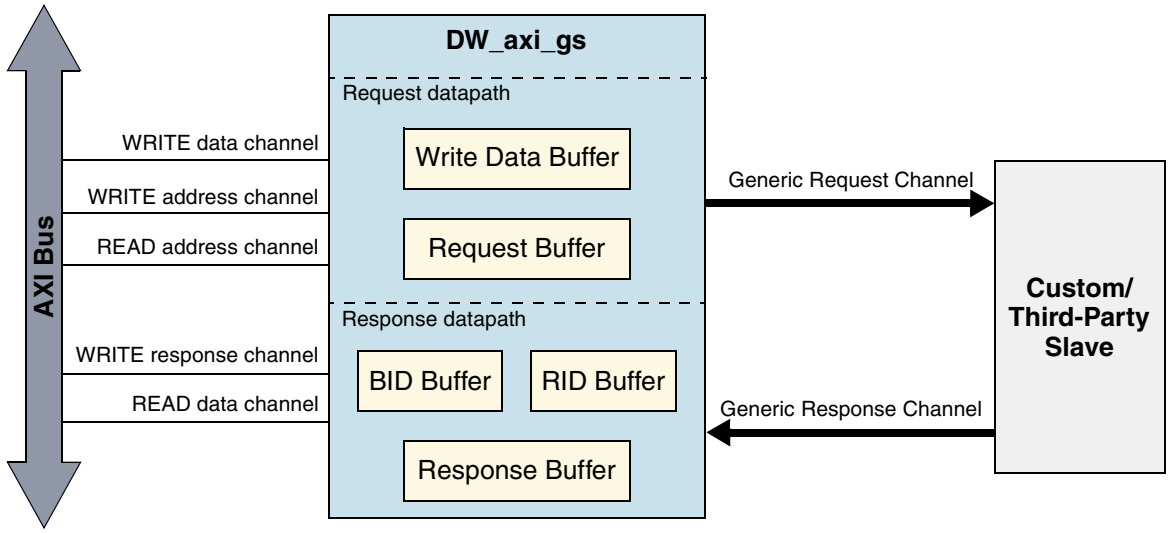
Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs

DW_axi_gs

AMBA AXI Slave to Generic Interface (GIF)

- Full support of the AXI protocol
- Configurable number of exclusive access monitors
- Full support of AXI low-power interface
- Two-way flow control
- Synchronous point-to-point communication on GIF
- Independent request and response GIF channels
- Configurable number of outstanding transactions
- Synchronous clock support; including slower GIF clock
- Configurable microarchitecture
- Configurable I/O signals to support simple peripherals



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

Documentation for this product is available at:

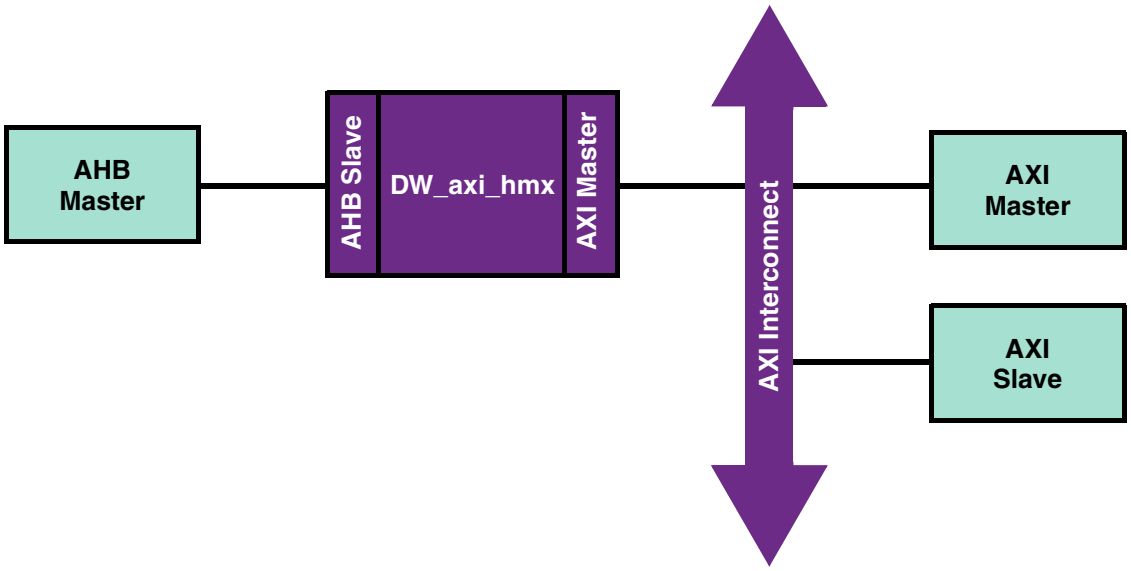
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_axi_hmx

Connects AMBA AXI Slave to AHB Master

- Connects a single AHB master to a single AXI slave without use of AHB bus fabric
- Single clock design with quasi-synchronous hclk
- Buffered write transactions
- Write error indication by hardware interface
- Low-power interface
- Big endian AHB-to-AXI conversion
- Locked transactions
- Support for all AHB burst types
- Timing mode options to ease timing closure
- Option to block writes
- Static setting of AWPORT/ARPORT secure bit



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

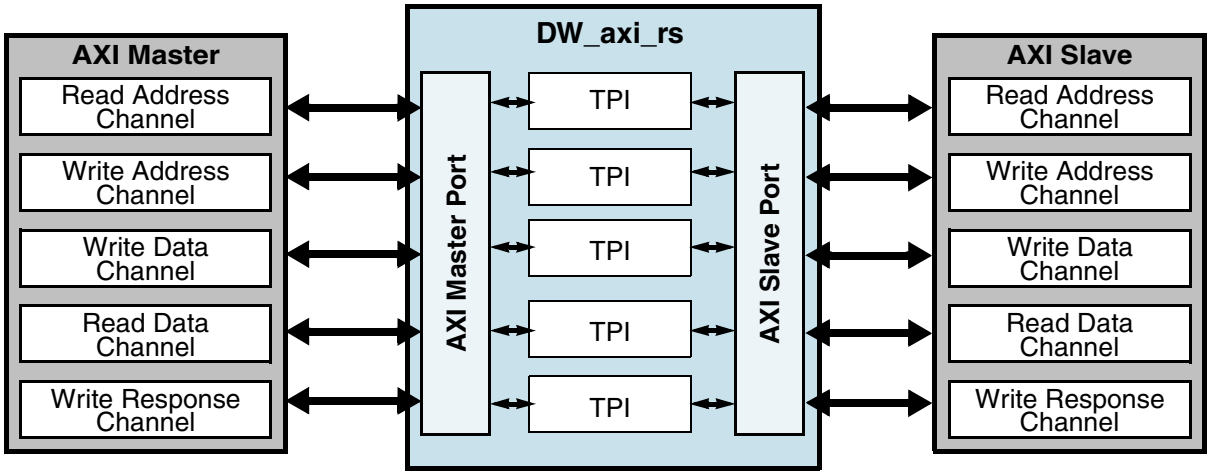
Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs

DW_axi_rs

AMBA AXI Register Slice

- Full support of the AXI protocol
- Supports the following timing modes:
  - Pass Through
  - Forward Registered
  - Fully Registered
  - Backward Registered
- Configurable timing mode option on a per channel basis. The timing mode option selected for a channel is independent of the option selected for the other AXI channels.
- No throughput penalty for any of the timing mode options
- Sideband signaling support
- Master and slave have same address width, data width, ID width, and burst width
- Same clock domain for attached master and slave
- Adds one cycle of latency on registered paths



This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

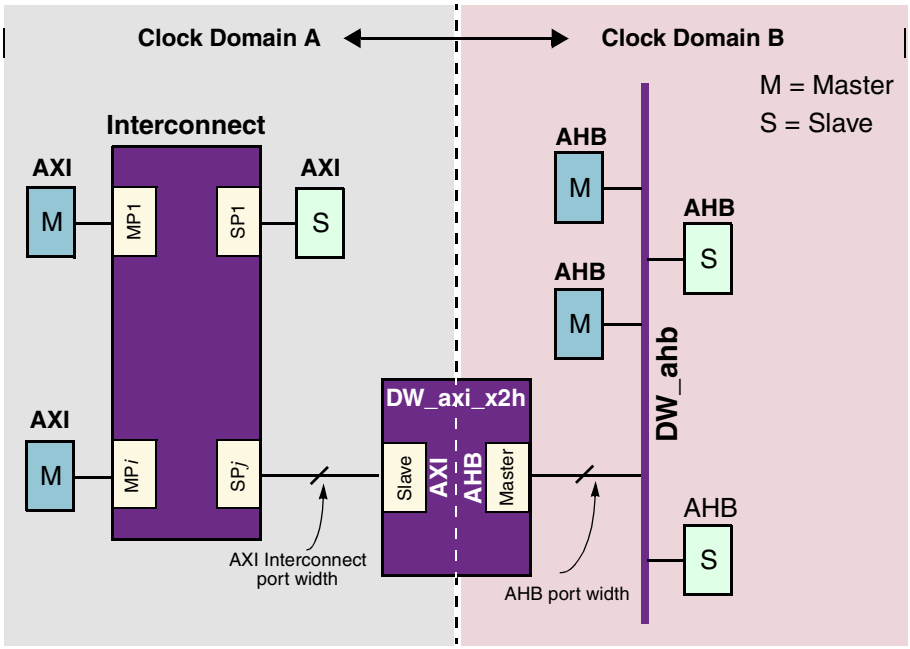
Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_axi_x2h
AXI to AHB Bridge

- Bridge from AXI to AHB bus, allowing for easy integration of legacy AHB designs with newer AXI designs
- Configurable AXI Slave interface
- Configurable AHB Master interface; includes AHB Lite support
- AMBA AXI and AMBA 2.0 (AHB) compliant
- Configurable depths on command, data, and response queues
- All transactions passed through industry-standard DesignWare FIFOs
- Supports transfer downsizing; AHB data width can be the same as AXI or narrower
- Configurable synchronous or asynchronous AXI/AHB clock operations with any clock ratio



This component is coreAssembler ready. For more information about coreAssembler, refer here:

http://www.synopsys.com/products/designware/core_assembler.html

The *DesignWare DW_axi_x2h Databook* is available at:

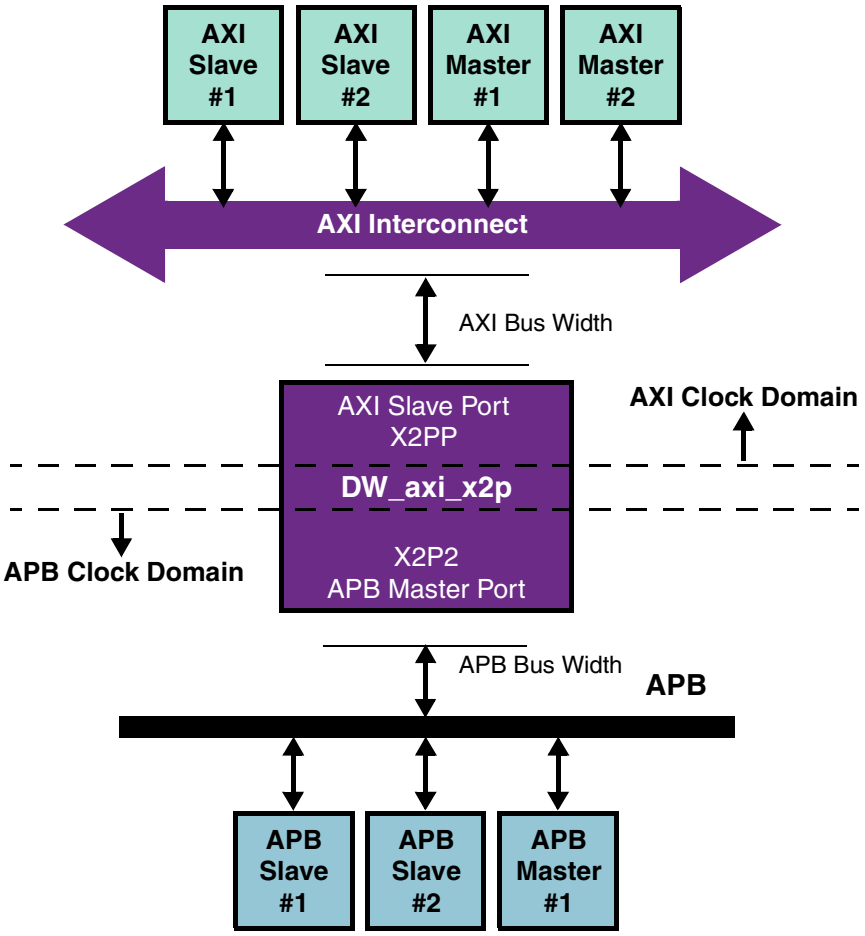
http://www.synopsys.com/products/designware/docs

AMBA Compliant

DW_axi_x2p

Connects AMBA AXI Slave to AHP Master

- Translates AXI transactions into APB transfers
  - Compliance with *AMBA 3 APB Protocol Specification*, Rev. 1.0 and AMBA AXI Protocol Rev. 1.0 from ARM
  - Configuration option for AMBA 2 (APB) compatibility
  - Accepts simultaneous read/write AXI transactions
  - APB attempts to honor AXI data transfer intent on each APB transfer.
- Support for different clock domains
  - Single clock or two clocks of any clock integer ratio
  - Support for quasi-synchronous clocking – single clock with the use of a pclk_enable allows APB side of bridge to issue at a slower rate than the system.
- Flexible address and data port configurations
  - AXI data ports: 8, 16, 32, 64, 128, 256, or 512 bits wide
  - APB data ports: 8, 16, or 32 bits wide
  - AXI address ports: 32 or 64 bits
  - APB address ports: 32 bits
  - AXI little or big endian byte ordering (byte invariant). APB is always little endian.
- Buffers AXI transactions
  - Buffers activity on all of the AXI channels, minimizing waits on AXI control, data, and response
  - Supports a wide range of user-selectable depths for the command queues, response buffer, read data, and write data buffers

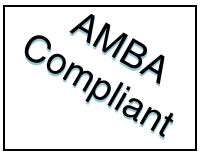


This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs



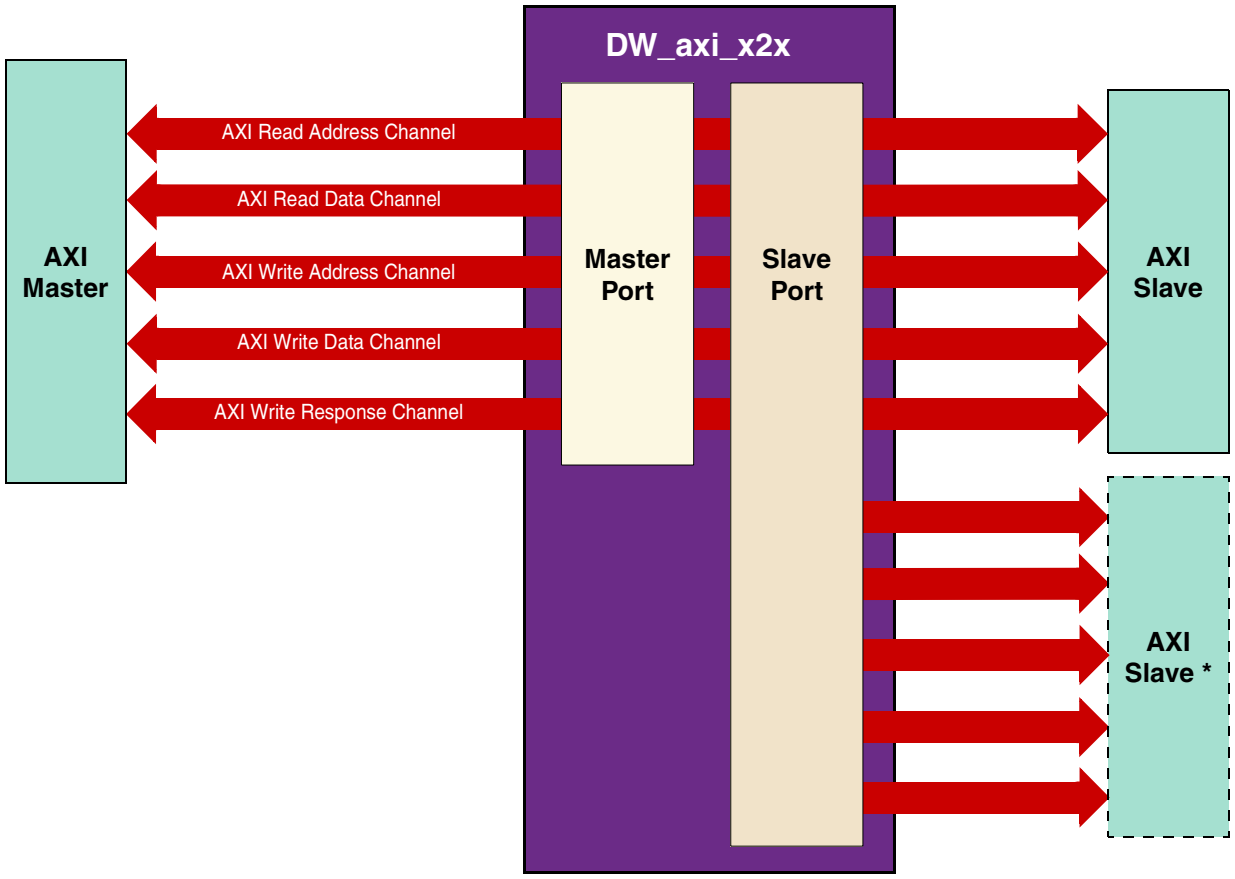
DW_axi_x2x

Connects AMBA AXI Master to AXI Slave

- Translates AXI transactions into APB transfers
  - Compliance with AMBA AXI Protocol Rev. 1.0 from ARM
  - Transparent Operation—transaction attributes altered when necessary to fit on secondary bus
  - Accepts simultaneous AXI transfers on all 5 channels; passes to primary/secondary AXI bus
  - Configurable buffer depths for all 5 channels to allow off-loading of payload source bus to sink bus
  - Support for asynchronous clocks on Slave Port and Master Port sides
  - Optimizations for quasi-synchronous clocking of any integer ratio
- Address Channel Features
  - Address width configurable to any value in range 32-64 on both Slave and Master Ports
  - Changes attributes for transactions that cannot fit on the secondary bus
  - For upsizing, increases SIZE of transaction and decreases length to generate transaction of SIZE equal to maximum on secondary bus
  - Configures which channels exist—write-only, read and write; allows for use in purely write interleaving fan-out mode
  - Supports burst lengths of up to 256
- Data Channel Features
  - Data Ports: 8, 16, 32, 64, 128, 256, 512 bits wide
  - Master Port and Slave Port data widths can be configured to different widths
  - Transfer unpacking done to translate larger Master Port data width to smaller Slave Port data width; on return from Slave Port to Master Port, transfers packed to match size of original transaction from primary bus
  - Can upsize transactions; that is, pack data from primary into shorter transaction of larger SIZE on secondary
  - AXI little- and big-endian Byte Ordering (byte invariant) is individually configurable for each interface
  - Configurable read interleaving depth; allows external slave to reorder and/or interleave read data up to this depth
  - Configurable write interleaving depth

DW_axi_x2x
Connects AMBA AXI Master to AXI Slave

AMBA Compliant



* Optional AXI Slave only with write interleaving fan-out

This component is coreAssembler ready. For more information about coreAssembler:

http://www.synopsys.com/products/designware/core_assembler.html

Documentation for this product is available at:

http://www.synopsys.com/products/designware/docs

DesignWare AMBA QuickStart

Collection of example designs for AMBA subsystems

DesignWare AMBA QuickStart is a collection of example designs for AMBA subsystems built with DesignWare AMBA On-chip Bus synthesizable IP and verification IP components. The QuickStart demonstrates the following:

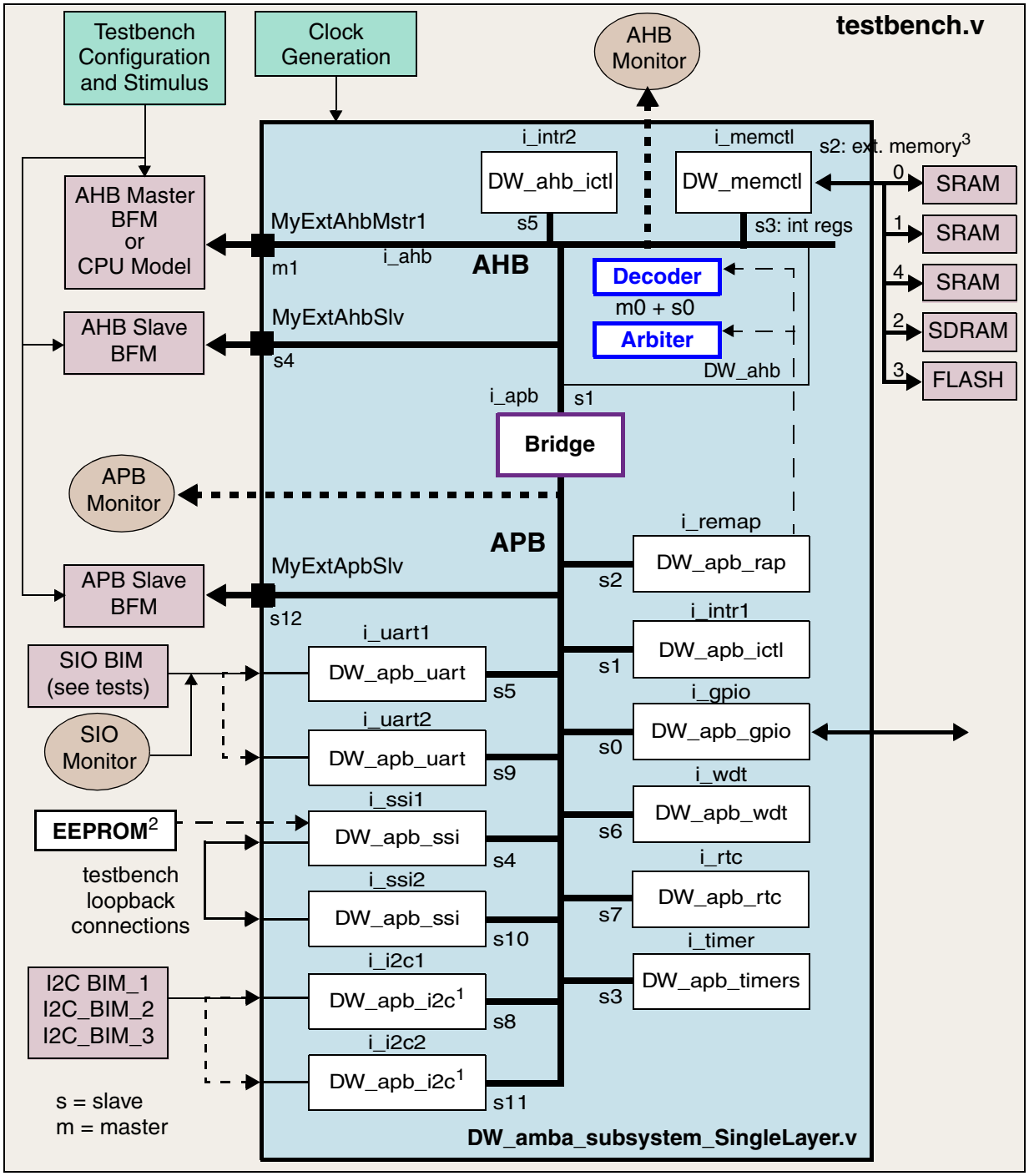
- How the DesignWare AMBA components and peripherals (synthesizable IP) integrate together.
- How to initialize and program (using C or Verilog BFM commands) the synthesizable component blocks to perform basic operating functions.
- How the DesignWare AMBA verification models and synthesizable components work together.
- How to connect and use a microprocessor model within a DesignWare AMBA subsystem.

QuickStart currently includes two example designs:

- QuickStart_SingleLayer – This is a single-layer subsystem. This subsystem is an enhanced version of the QuickStart example that was included in the DesignWare AMBA 2004.05 release.
- QuickStart_MultiLayer – This is a multi-layer subsystem with DMA, PCI, USB, ICM, AHB-bridge and other peripheral components.

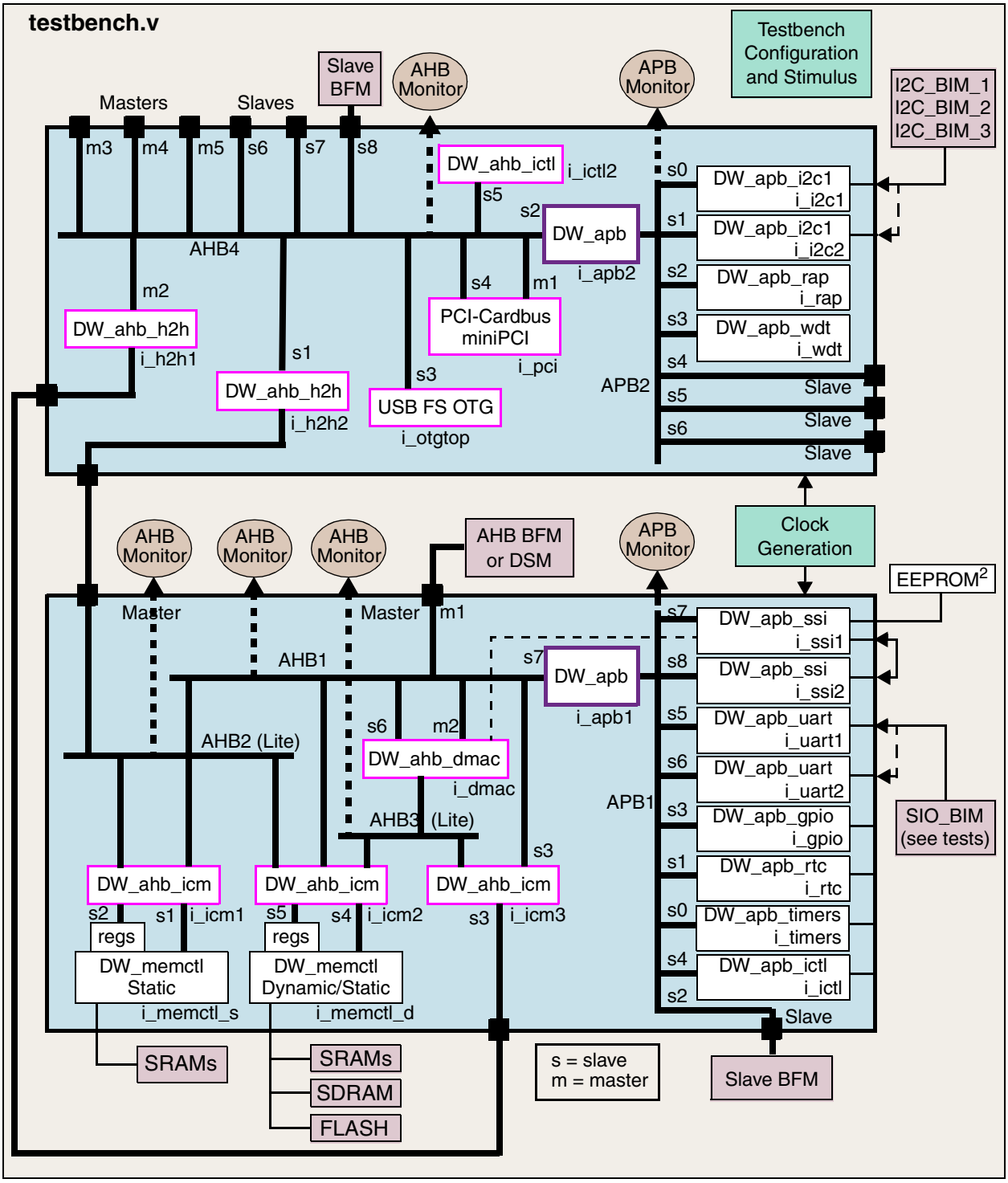
The QuickStart_SingleLayer and QuickStart_MultiLayer subsystems include pre-configured instances of DesignWare AMBA Bus IP and peripheral components as shown in the following figures, respectively.

For more information about using DesignWare AMBA QuickStart, refer to the *DesignWare AMBA QuickStart_SingleLayer Guide* and the *DesignWare AMBA QuickStart_MultiLayer Guide*.



2 DW_apb_ssi (i_ssi1) can also communicate with an EEPROM as opposed to the other DW_apb_ssi (i_ssi2).

3 DW_memctl (i_memctl) connects to five external memories: three SRAMs, one SDRAM, and one FLASH.



2 The DW_apb_ssi component (i_ssi1) in the example subsystem can also communicate with an EEPROM as opposed to another DW_apb_ssi (i_ssi2).

Memory IP

The following Memory IP are briefly described in this section:

Component Name	Component Description	Component Type
DW_memctl	Memory Controller (page 65)	Synthesizable RTL
DW_rambist	DesignWare Memory BIST solution (page 67)	Synthesizable RTL

To view the complete DesignWare memory portfolio, refer to the following:

http://www.synopsys.com/products/designware/memorycentral

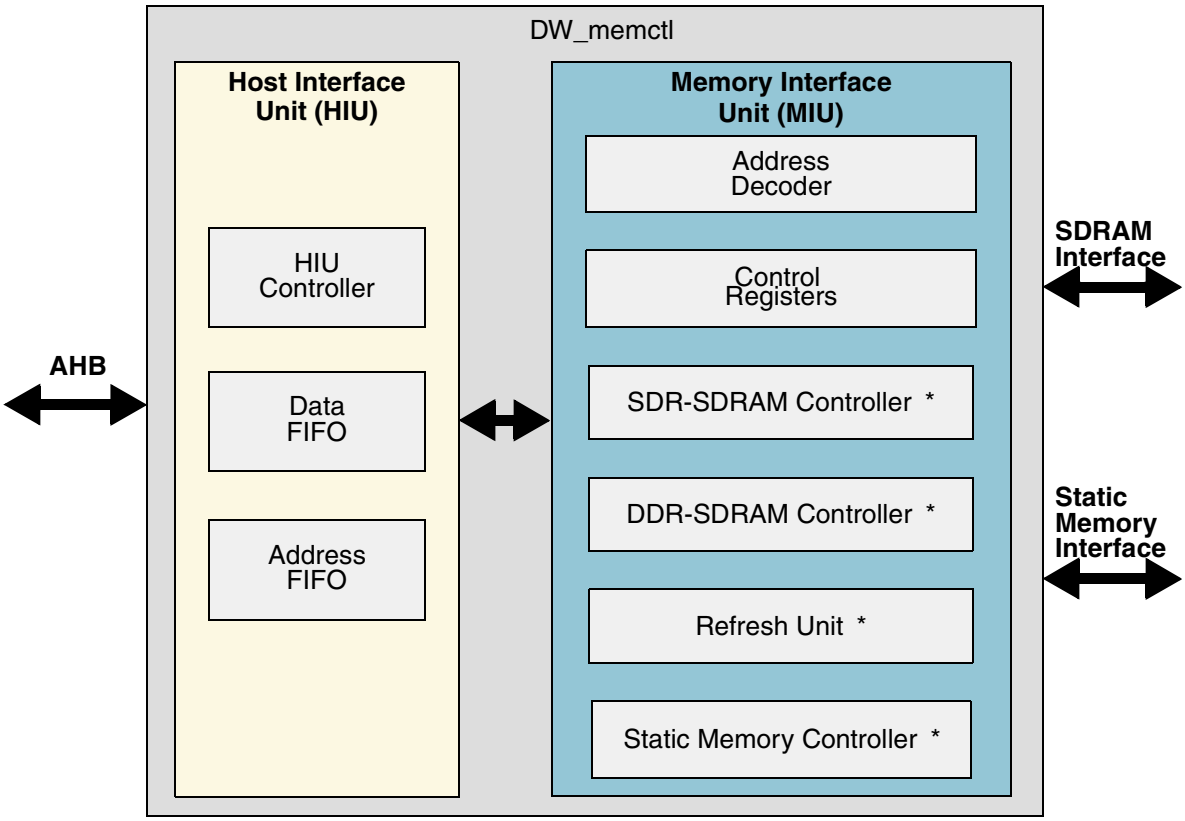
AMBA Compliant

DW_memctl
Memory Controller

- Supports AHB data widths of 32, 64, or 128 bits, AHB address width of 32 bits
- Supports pin-based little- or big-endian modes of operation
- Supports separate or shared memory address and/or data buses between SDRAM and Static memories
- Glueless connection to all JEDEC-compliant SDRAM
- Supports up to 16 SDRAM address bits
- SDR-SDRAM, Mobile-SDRAM, and SyncFlash memory data widths: 16, 32, 64, or 128, with 1:1 or 1:2 ratios with AHB data width.
  DDR-SDRAMs, memory data width: 8, 16, 32, or 64,with 1:2 or 1:4 ratios with the AHB data width.
- Programmable row and column address bit widths
- Supports 2K to 64K rows, 256 to 32K columns, and 2 to 16 banks
- Supports up to 8 chip selects, with a maximum of 4 GB of address space per chip select
- Supports asynchronous SRAMs, page-mode FLASHes and ROMs
- Supports up to three sets of timing registers
- Supports external “READY” handshake pin to interface non-SRAM-type device

Note: Does not generate split, retry, or error responses on the AHB bus

Also see the block diagram on the following page.



Note: * Conditional Instantiations

The *DesignWare DW_memctl MacroCell Databook* is available at:

http://www.synopsys.com/products/designware/docs

DW_rambist

Memory Built-In Self Test

Interfaces

- IEEE 1149.1 TAP controller interface
- Two clock interface, one for a slower TAP I/F, second for at-speed BIST execution
- Optional MUX block that supports either embedded multiplexers inside the memories or user-specified multiplexers
- Flexible configuration for embedded MUX block, providing a better interface to memory control signals with different widths and polarities

Error Diagnostics

- Pause on first and subsequent failures mode, serial debugging
- Failing address and data may be scanned out for examination
- Quick debug mode, continue on failures mode, failing addresses not recorded
- Parallel debug port to observe the failing memory data bits

BIST Tests

- User choice of March LR (14n), March C– (10n) and MATS++ (6n)
- Custom (user-defined) patterns option
- Optional SRAM retention test, (5n + delay), auto pause mechanism
- Selection of background and complement background data patterns
- Default sequence or run-time selection of individual test
- Improved test execution time through reduced memory read/write cycles (each access to synchronous memory occurs in one clock cycle)
- Configuration of Mode Register reset value to provide easy power-up tests
- Higher speed clock frequency

Supported Memories

- Synchronous and asynchronous SRAM
- Asymmetrical pipelining support, up to four stages
- Support for 32 memories per BIST controller
- Highly configurable memory interface to suit most types of memories

Supported Memory Configurations

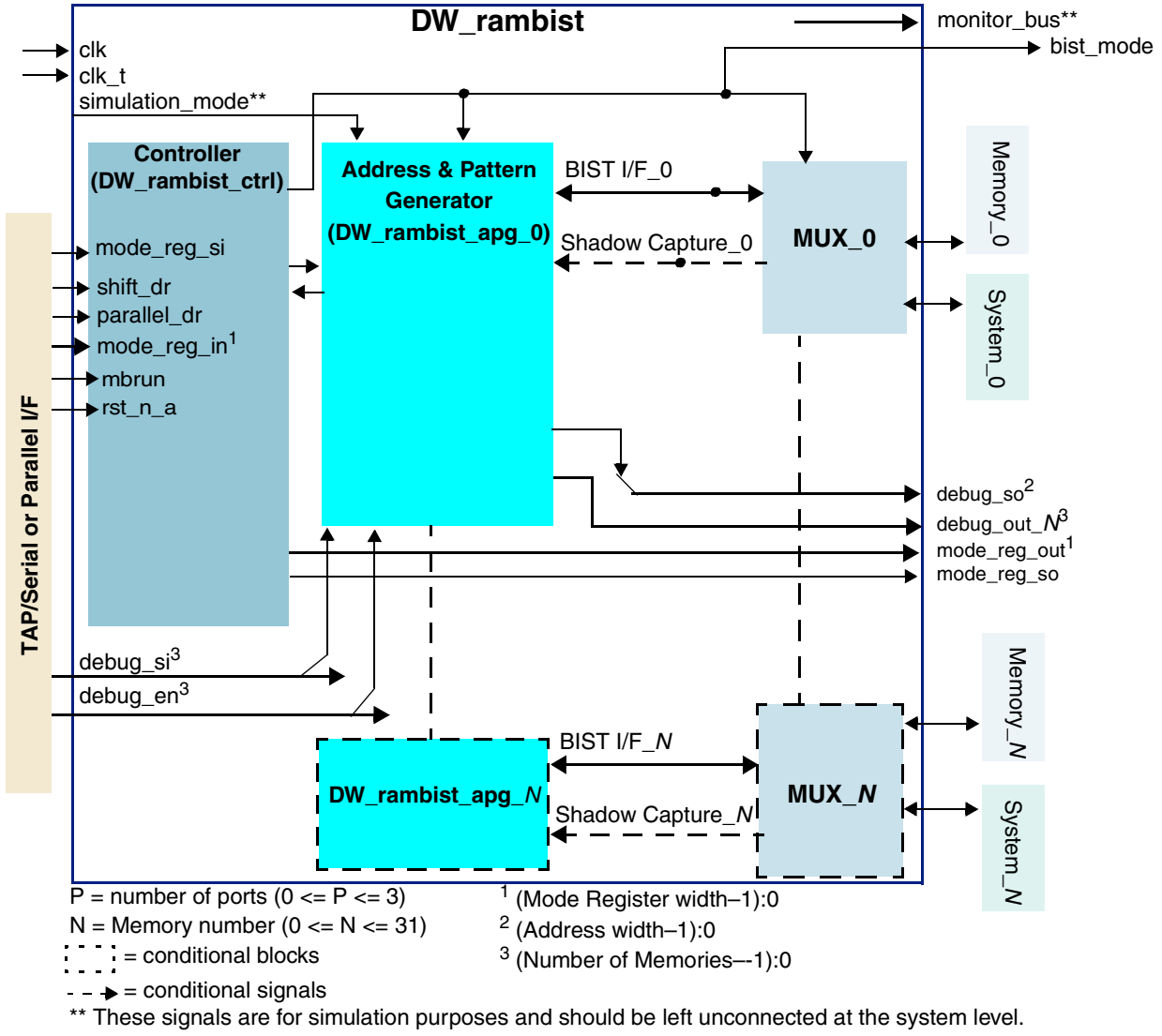
- True at-speed testing of memories in parallel
- Memory array test via single port and multi-port
- Ability to enable/disable testing of individual memories
- Multiple controller scheduling
- Support for incomplete address space

Design for test

- Configuration of shadow logic capture
- Sample script for scan chain creation and connection (part of example design)
- Integration with DFT Compiler, BSD Compiler, and TetraMax

Design for Verifiability

- simulation_mode signal to provide verification of very large configurations and to quickly check system-level interconnection



More information on the DW_rambist MacroCell can be found at:

http://www.synopsys.com/products/designware/docs/ds/i/DW_rambist_ds.pdf

Microprocessors/Microcontrollers

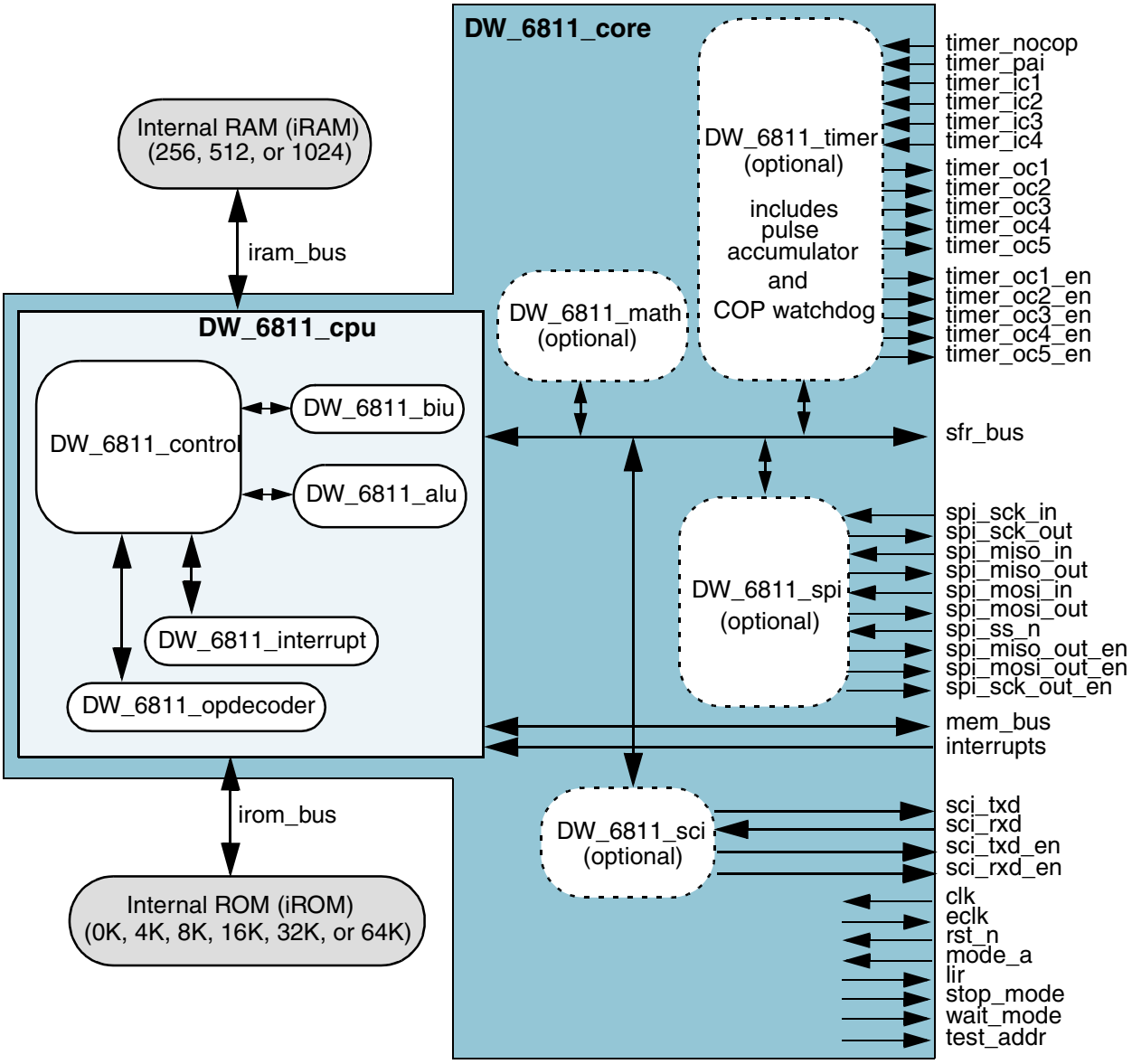
The components detailed in this section contain a page reference in the following table.

Component Name	Component Description
DW_IBM460-S, DW_IBM405-S [a]	PowerPC 440 Microprocessor Core from IBM (page 177)
DWC_n2p	Nios II Processor Core (page 182)
DW_6811	8-bit Microcontroller (page 70)
DW8051	8-bit Microcontroller (page 72)

a. Synthesizable RTL of the processor cores are available through the Star IP Program. For more information on this program, visit http://www.synopsys.com/designware.

DW_6811
6811 Microcontroller

- Compatibility with industry standard 68HC11 microcontroller:
  - 8-bit CPU with 8-bit/16-bit ALU:
    - Two 8-bit accumulators that can be concatenated to provide 16-bit addition, 16-bit subtraction, 16 x 16 division, 8 x 8 multiplication, shift, and rotate
    - Up to 18 maskable interrupt sources (17 maskable internal interrupts and 1 maskable external interrupt)
    - Power saving STOP and WAIT modes
  - Standard 68HC11 instruction set
- Simple integration of user-defined peripherals through external Special Function Register (SFR) interface, within SFR array space
- Fully synchronous implementation
- A BIU unit to provide control signals for memory and I/O ports:
  - Programmable memory map for internal RAM (iRAM) and SFR array spaces.
  - Parameterized internal ROM (iROM) size
  - De-multiplexed external memory interface
- Optional peripherals:
  - 16-bit timer
    - Three Input Capture (IC) channels
    - Four Output Compare (OC) channels
    - One software selectable IC or OC channel
  - 8-Bit pulse accumulator
  - COP watchdog timer system
  - SPI synchronous serial port, basic or enhanced (SPI or SPI+)
  - SCI UART, basic or enhanced (SCI or SCI+)
  - Up to 3 external reset/interrupt sources
  - Up to 17 internal interrupt sources



The *DesignWare DW_6811 MacroCell Databook* is available at:

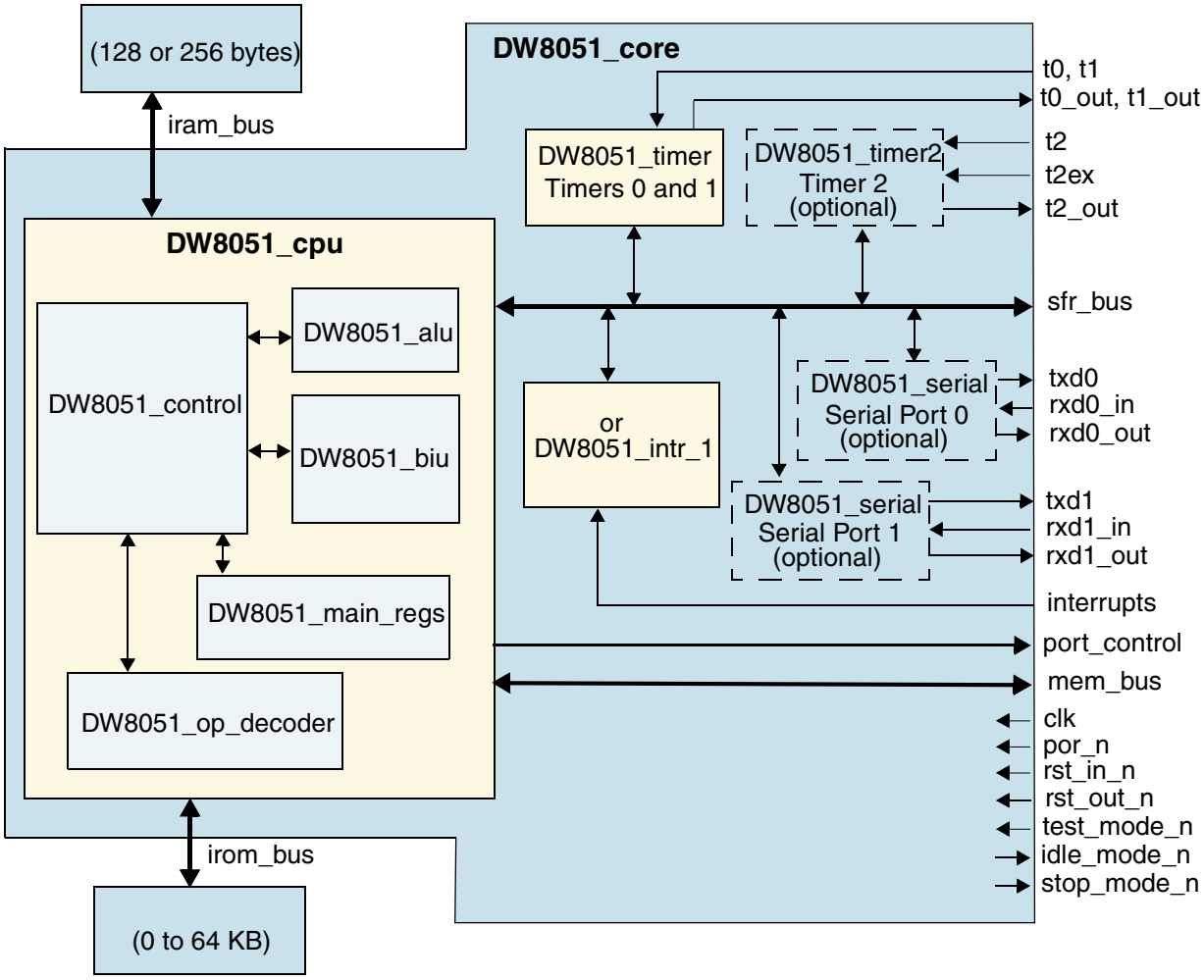
http://www.synopsys.com/products/designware/docs

MacroCells

DW8051

8051 Microcontroller

- Compatible with industry-standard 803x/805x:
  - Standard 8051 instruction set
  - Optional full-duplex serial ports selectable through parameters
  - Optional third timer selectable through parameter
  - Control signals for standard 803x/805x I/O ports
- High–speed architecture:
  - Four clocks per instruction cycle
  - 2.5X average improvement in instruction execution time over the standard 8051
  - Runs greater than 300 MHz in 90 nanometer process technology.
  - Wasted bus cycles eliminated
  - Dual data pointers
- Parameterizable internal RAM address range
- Parameterizable internal ROM address range
- Simple integration of user-defined peripherals through external Special Function Register (SFR) interface
- Enhanced memory interface with 16-bit address bus
- Variable length MOVX to access fast/slow RAM peripherals
- Fully static synchronous design



The *DesignWare DW_8051 MacroCell Databook* is available at:

http://www.synopsys.com/products/designware/docs

2 DesignWare Library Verification IP

Overview

The following table identifies the various components that make up the DesignWare Library's Verification IP offering. See page 81 for a listing of the Board Verification IP component groups. DesignWare Verification IP can also be licensed individually and is available as part of the VCS Verification Library.

Component Name	Component Description	Model Technology
DesignWare Bus & I/O Standards		
ahb_bus_vmt, ahb_master_vmt, ahb_monitor_vmt, ahb_slave_vmt	DesignWare VIP for AMBA 2.0 AHB Models (page 76)	VMT
apb_master_vmt, apb_monitor_vmt, apb_slave_vmt	DesignWare VIP for AMBA 2.0 APB Models (page 78)	VMT
axi_master_vmt axi_slave_vmt axi_monitor_vmt axi_interconnect_vmt axi_port_monitor_vmt	DesignWare VIP for AMBA 3 AXI (page 79)	VMT
ethernet_txrx_vmt, ethernet_monitor_vmt	10/100/1G/10G Ethernet Models (page 82)	VMT
enethub_fx, rmiirs_fx	Ethernet RMII Transceiver and Hub (page 83)	FlexModels page 96
i2c_txrx_vmt	I^2C Bi-Directional Two-Wire Bus (page 84)	VMT

pcie_txrx_vmt, pcie_monitor_vmt	PCI Express 2.0 protocol (page 88)	VMT
pcimaster_fx, pcislave_fx, pcimonitor_fx	PCI/PCI-X Simulation Models and Test Suite (page 90)	FlexModels page 96
sata_device_vmt sata_monitor_vmt	Serial ATA Models (page 92)	VMT
sio_txrx_vmt, sio_monitor_vmt	Serial Input/Output Interface Models (page 94)	VMT
usb_host_vmt, usb_device_vmt, usb_monitor_vmt	USB On-The-Go Models, 1.1, 2.0, OTG, UTMI, and UTMI+ (page 95)	VMT
DesignWare Design Views of Star IP Microprocessors and DSP Core		
DW_IBM460-S, DW_IBM405-S	PowerPC 440 32-Bit Microprocessor Core from IBM (page 177)	Compiled model
DW_CoolFlux	CoolFlux 24-bit DSP Core from NXP (page 179)	Compiled model
DesignWare Memory - Access to the full suite of memory IP is made available through DesignWare Memory Central; a memory-focused Web site that lets designers download DesignWare Memory IP and documentation. Visit Memory Central at: http://www.synopsys.com/products/designware/memorycentral		Memory Models
SmartModel Library is a collection of over 3,000 binary behavioral models of standard integrated circuits supporting more than 12,000 different devices.		SmartModels page 98

Verification Models

The following datasheet pages are ordered alphabetically and briefly describe each Verification Model.

Verification IP

DesignWare AMBA AHB Models

Master, Slave, Monitor, Bus Interconnect

All Models

- Multiple command streams
- Verilog, VHDL, or OpenVera testbenches
- Configurable message formatting
- Event-driven testbenches
- Support VCS Native Testbench (NTB)
- Support OpenVera Reference Verification Methodology (RVM)
- Support *Verification Methodology Manual* (VMM) for SystemVerilog

AHB Master (ahb_master_vmt)

- Data width: 8-1024 bits
- Single or burst transfers
- Burst rebuild capability
- Constrained random test transactions using random, file, memory, or FIFO data
- Compare with expected data

AHB Slave (ahb_slave_vmt)

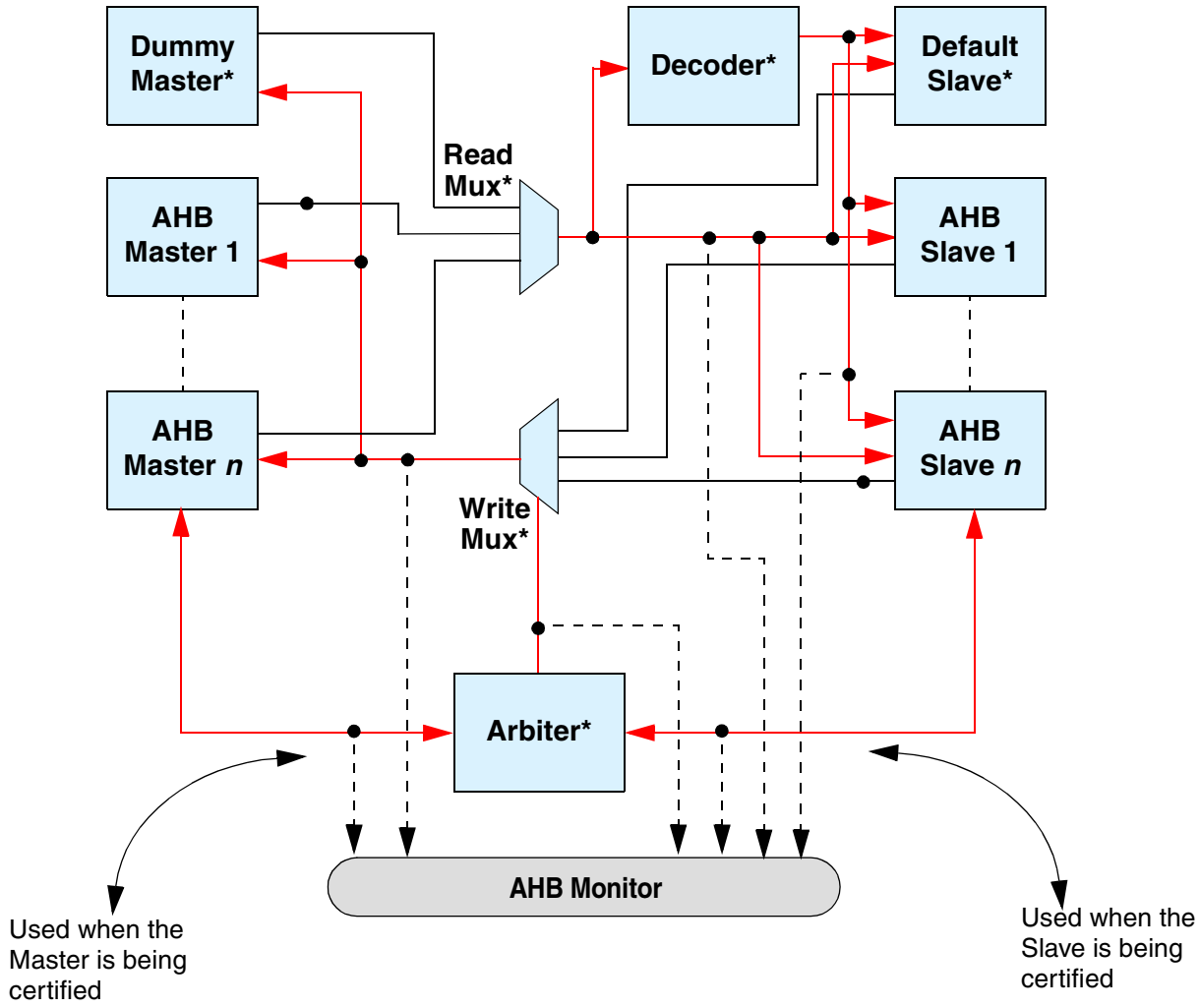
- OK, Error, Retry, or Split responses
- Programmable wait states
- Configurable memory fill patterns
- FIFO memory at any memory location
- Constrained random test transactions using random, file, memory, or FIFO data

AHB Monitor (ahb_monitor_vmt)

- Cycle-based or transaction-based event monitoring
- Protocol checking
- Incremental coverage reporting

AHB Bus Interconnect (ahb_bus_vmt)

- Up to 15 Masters and 15 Slaves
- Unlimited Slave memory maps
- Priority-based arbitration algorithm
- All types of Master transfers
- All types of Slave responses
- Configurable early burst termination and undefined length burst termination



* Dummy Master, Default Slave, Arbiter, Decoder, Write Mux, and Read Mux are part of the AHB Bus VIP model.

The *DesignWare AHB Verification IP Databook* is available at:
http://www.synopsys.com/products/designware/docs

Verification IP

DesignWare AMBA APB Models

Master, Slave, Monitor

All Models

- Multiple command streams
- Verilog, VHDL, or OpenVera testbenches
- Configurable message formatting
- Event-driven testbenches
- Support VCS Native Testbench (NTB)
- Support OpenVera Reference Verification Methodology (RVM)
- Support *Verification Methodology Manual* (VMM) for SystemVerilog

APB Master (apb_master_vmt)

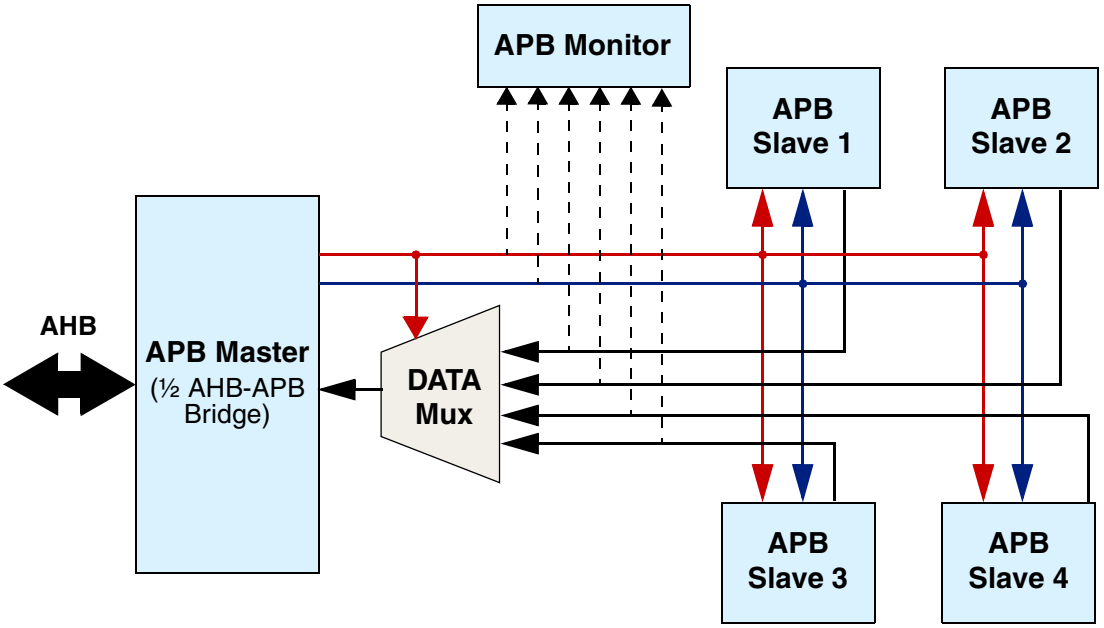
- 1-16 Slaves
- Data/Address width: 8-32 bits
- Constrained random test transactions using random, file, memory, or FIFO data
- Internal or external data mux
- Error injection capability

APB Slave (apb_slave_vmt)

- Data/Address width: 8-32 bits
- Configurable memory fill patterns
- Big endian or little endian
- FIFO memory at any memory location

APB Monitor (apb_monitor_vmt)

- Transaction logging
- Protocol checking
- Incremental coverage reporting



The *DesignWare APB Verification IP Databook* is available at:
http://www.synopsys.com/products/designware/docs

DesignWare VIP for AMBA 3 AXI

Master, Slave, Monitor, Interconnect

All Models

- Compliant with AXI 1.0 specification
- Support all AXI data/address widths
- Support all protocol transfer types and response types
- Checks for all protocol violations
- Logs transactions and reports on protocol coverage
- Configurable message formatting
- Support VCS Native Testbench (NTB)
- Support OpenVera Reference Verification Methodology (RVM)
- Support *Verification Methodology Manual* (VMM) for SystemVerilog

AXI Master (axi_master_vmt)

- Configurable outstanding transactions
- Out-of-order transaction completion
- Unaligned data transfers using byte strobes
- Protected accesses and Atomic access
- Response through command and notification

AXI Slave (axi_slave_vmt)

- Configurable multiple transaction
- Out-of-order completion
- Read interleaving
- Unaligned data transfers using byte strobes
- Variable Slave response
- Supports FIFO memory
- Slave aliases up to 3 additional portsResponse through notification at the end of Read/Write transactions

AXI Bus Monitor (axi_monitor_vmt)

- Full protocol checking for AXI interface protocol
- Up to 32 Master and 32 Slave ports
- Independent of interconnect support for shared buses
- Shared address-shared data, SASD
- Configurable data bus widths
- Configurable ID bus widths
- Master ID ports configure from 1-8 bits
- Slave ID ports configure from 1-13 bits
- Includes checks on channel handshake ordering
- Includes run-time control of checkers
- Transaction logging for AXI
- Supports configurable coverage analysis and reporting
- Automated coverage

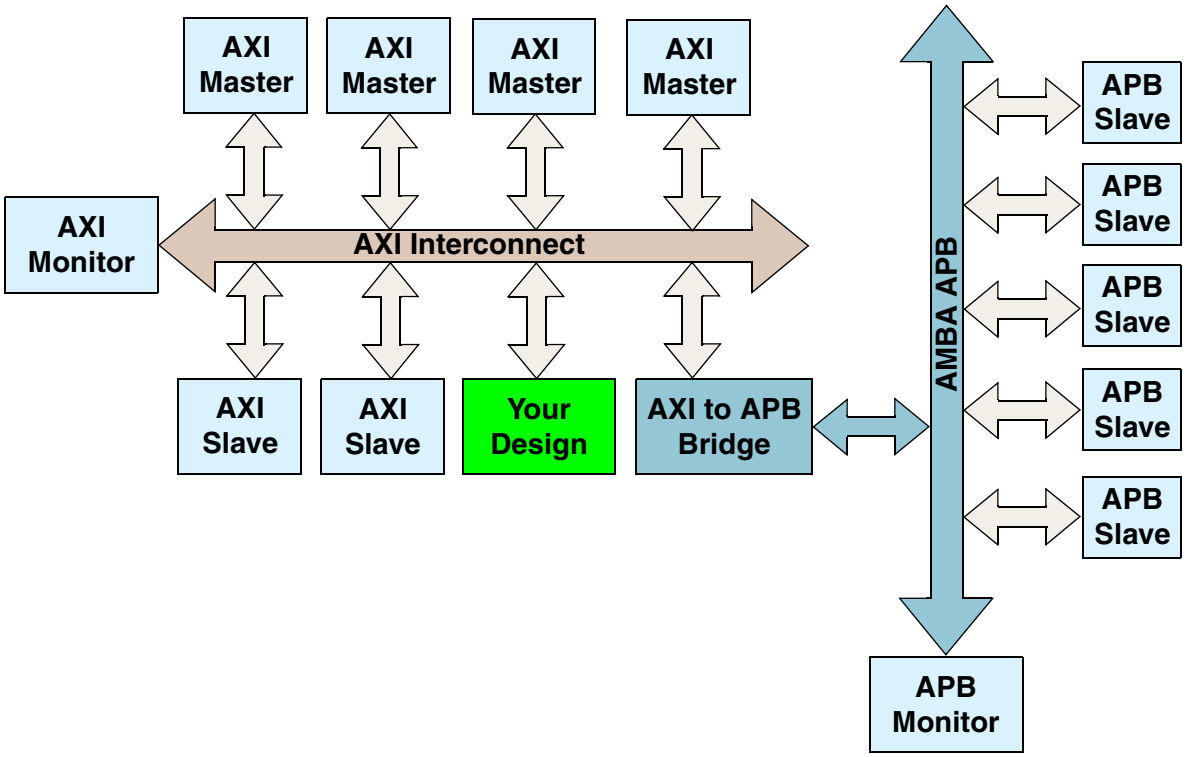
AXI Interconnect (axi_interconnect_vmt)

- Shared address-shared data, SASD
- Arbiter and Decoder on each channel bus
- Default Slave device supported
- Up to 32 Masters and 32 Slaves
- Configurable system address bus of 32 or 64 bits
- Configurable data bus up to 1024 bits
- All type of responses supported including burst and atomic access
- Unlimited memory map for each Slave.
- Pipelined operation on each channel with input-stage concept

AXI Port Monitor (axi_port_monitor_vmt)

- Interface to a single AXI port
- Multiple instantiations
- Supports any number of ports (more than 64) by using multiple independent instances
- Independent of bus architecture (multiple address/data channels)
- ID ports configurable from 0 to 32 bits
- Complete AXI Protocol checking
- Run time control of protocol checking
- Transaction logs
- Predefined coverage
- Sideband support that allows expansion to AXI protocol

Using the DesignWare Verification Models for the AMBA 3 AXI Interface is available at:
http://www.synopsys.com/products/designware/docs



Board Verification IP

Simulation models for Board Verification

The DesignWare Library contains over 18,500 simulation models for ASIC, SoC, and Board verification. For a complete search, visit http://www.synopsys.com/ipdirectory.

Component Group	Component Reference
VMT Models	Refer to "DesignWare Library Verification IP" on page 74
FlexModels	Refer to "DesignWare FlexModels" on page 96
DesignWare Memory Models	Refer to "Memory Models" on page 85
SmartModel Library	Refer to "DesignWare SmartModels" on page 98

Ethernet (10, 100, 1G, 10G) Models

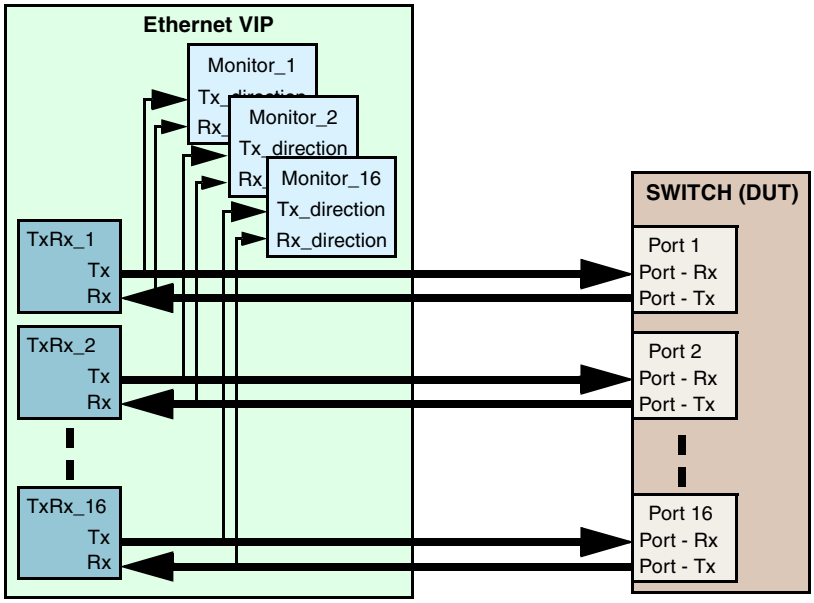
Transceiver and Monitor

Transceiver (ethernet_txrx_vmt)

- Interfaces for 10, 100, 1G, and 10G (XGMII, XAUI, MII, GMII, SMII, SGMII, QSGMII, RMII, RGMII, 1000BASE-KX, 10GBASE-KR, and 10GBASE-KX4, TBI, RTBI)
- Half and full duplex MAC operation
- Multiple frame types (MAC, VLAN tagged, control, and jumbo)
- Auto-Negotiation for SGMII and TBI
- User-defined frame content
- Flow control with Pause frames
- Adjusts IPG for effective data rate
- Frame error generation and recognition
- Code error generation/injection
- Link fault support
- IEEE 1588 Precision Clock
- IEEE 802.3ap Backplane Ethernet
- Supports VCS NTB and *Verification Methodology Manual* (VMM) for SystemVerilog and OpenVera (RVM)

Monitor (ethernet_monitor_vmt)

- Protocol checking for supported frame types and errors
- Transaction logging for frames, fault messaging, and cycle-level bus activity
- Configurable to match TxRx model
- Watchpoint monitoring
- Cumulative simulation coverage
- Dynamic start/stop
- Command set control
- Supports VCS NTB
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog and OpenVera (RVM)



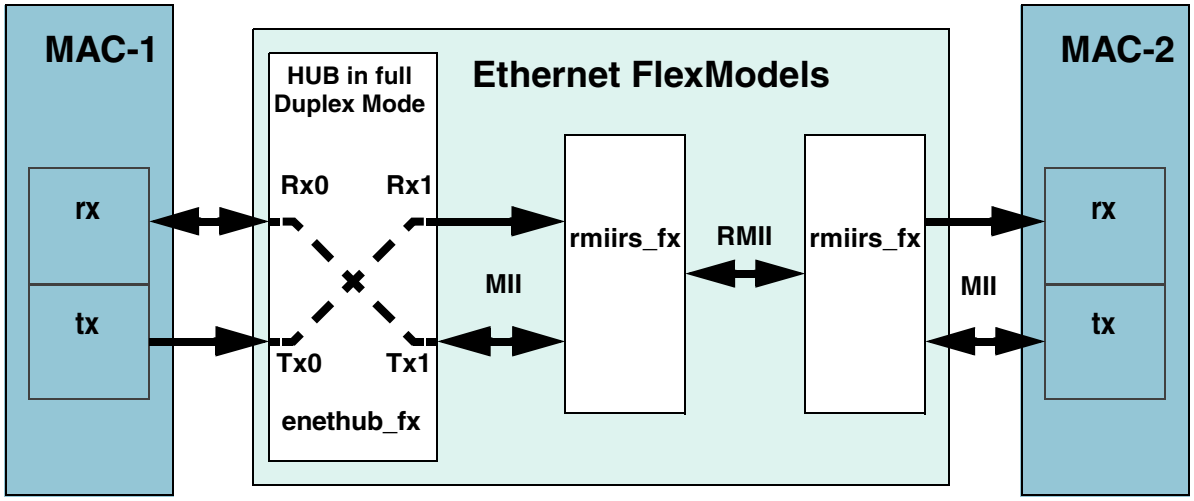
The *DesignWare Ethernet Verification IP* documentation is available at:
http://www.synopsys.com/dw/doc.php/vip/ethernet/latest/doc/ethernet__overview.pdf

Ethernet Models

RMII Transceiver and Hub

The Synopsys Ethernet FlexModel set consists of two models and system testbenches in OpenVera, Verilog, C, and VHDL.

- **rmiirs_fx**. The RMII interface is a low pin count MII interface intended for use between the ethernet PHY and switch (or repeater) ASICs. The interface has the following features: supports 10 Mb/s and 100 Mb/s data rates. single clock reference is sourced from the MAC to PHY (or from an external source); and, independent 2-bit wide transmit and receive paths.
- **enethub_fx**. This FlexModel is the BFM that supports hub functionality for the MII, MII 100 and GMII Ethernet MAC. The following types of operations are performed by the model: acts as a common PHY for all MACs connected on its MII ports, and propagates the transmitted data from the transmitting MAC to all the MACs in the system.



The individual DesignWare FlexModel databooks can be found with each model at:

http://www.synopsys.com/products/designware/ipdir

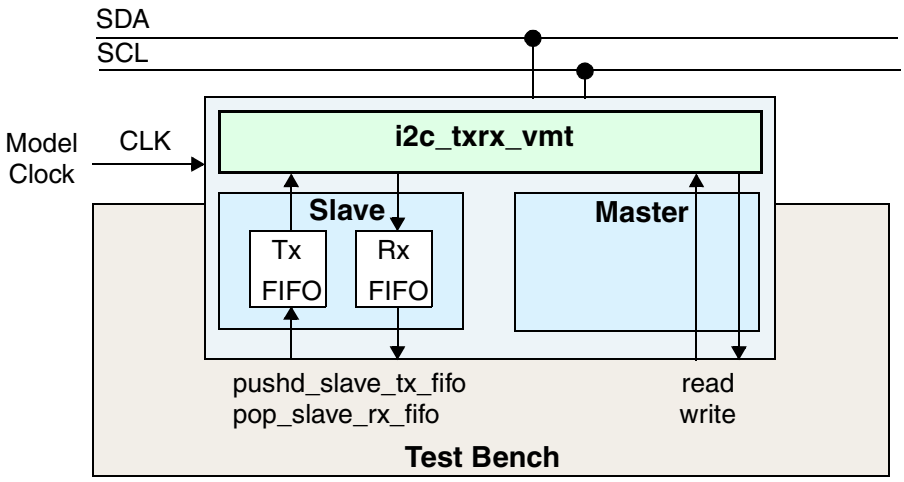
Verification IP

I²C Model

Transceiver

i2c_txrx_vmt Model

- Full I²C Master and Slave functionality
- Start, repeat start and stop for all possible transfers
- Supports all I²C clocking speeds
- 7b/10b configurable slave address
- Configurable Slave FIFOs allows testing of varied bus traffic patterns
- Supports VCS Native Testbench (NTB)
- Supports the Reference Verification Methodology (RVM)
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog
- Multiple command streams allow Slave and Master to operate concurrently
- Compares read data with expected results
- Bus-accurate timing
- Notifies the testbench of significant events such as transactions, warnings, and protocol errors.



The *DesignWare I²C Verification IP Databook* is available at:
http://www.synopsys.com/products/designware/docs

Memory Models

Simulation models of memory devices

DesignWare Memory Models are pre-verified simulation models of memory devices. The DesignWare Memory Models are built on top of the Synopsys memory model technology thus ensuring model accuracy, quality and reliability. With thousands of pre-verified memory models to choose from, supporting over 30 memory vendors, it's very easy to find a match to a systems' memory requirement.

The models integrate with the simulator through the de facto industry standard SWIFT interface, which is supported by all Synopsys simulators and by all other major simulator vendors. Smarter verification is achieved by using the models debugging utilities.

You can search through the thousands of memory models using the memory model search capabilities offered as part of DesignWare Memory Central at: http://www.synopsys.com/memorycentral.

DesignWare Memory Models provide the following capabilities:

- The DesignWare Memory Models all have built in memory debug utilities. The debug utilities can be controlled from a VHDL, Verilog, OpenVera or SystemC testbench. The verification engineer has access to memory load, dump, peek, poke and trace commands.
- Debugging the memory model content interactively during run-time simulation reduces the effort required to debug memory subsystems. The DesignWare MemScope allows users to view and modify all the memory model data, as well as monitoring the transaction types taking place on the selected models. The MemScope connects directly to the DesignWare Memory Model technology core and not through the simulator. This results in no simulation performance degradation even with the MemScope connected.
- The memory transaction history can be viewed dynamically during simulation or in a post processing fashion. The address and data fields can be searched to locate selected values quickly.
- The memory model content can be viewed or modified dynamically during the simulation. The data contents can be saved to a file for use as a pre-load file in subsequent simulations.

The Memory Model documentation is available at:

http://www.synopsys.com/products/designware/docs

Open Core Protocol (OCP) Models

Master, Slave, and Monitor

All Models

- Full range of OCP configurations
- Multi-threading and bursts
- Configure as core or system
- Example VMM testbench with predefined test sequences and scenario generators to provide functional coverage of OCP 2.0, 2.1, or 2.2
- Randomized stimulus generation and configuration
- Generates logs and reports to observe OCP transactions
- Multiple testbench language support—SystemVerilog, Verilog, VHDL
- Supports all major simulators
- Supports Native Testbench (NTB) in VCS and VCS-MX
- Supports Verification Methodology Manual (VMM) for SystemVerilog testbenches
- Includes a utility to create OCP trace files for postprocessing

OCP Master Model (ocp_master_svt)

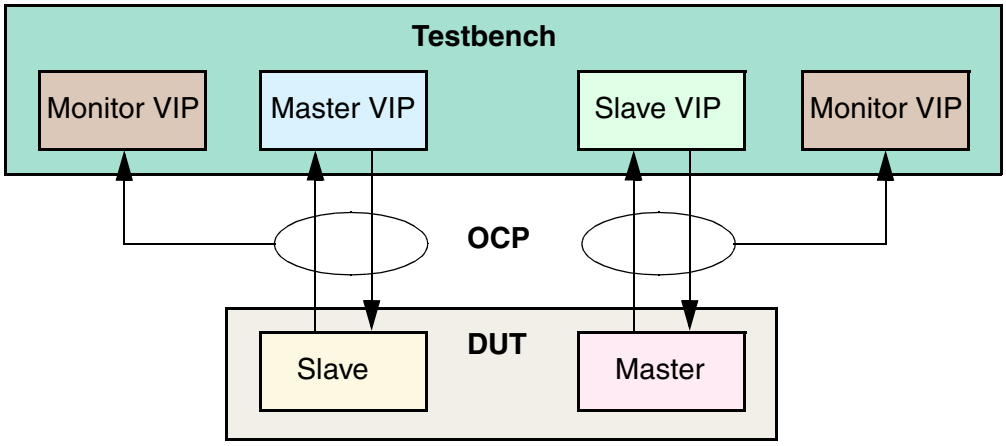
- Initiates OCP dataflow transactions
- Initiates and responds to activity on sideband signals
- Can be set up as an OCP core or system master

OCP Slave Model (ocp_slave_svt)

- Automatically manages responses to dataflow transactions
- Slave's response can be generated randomly or supplied from the testbench
- May initiate and respond to activity on the sideband and signals
- Can be set up as an OCP core or system slave

OCP Monitor Model (ocp_monitor_svt)

- Observes dataflow transactions and control signals
- Generates log files and coverage reports to track verification progress
- Log files show a record of observed transactions
- Functional coverage reports


Testbench
Monitor VIP
Master VIP
Slave VIP
Monitor VIP
OCP
DUT
Slave
Master

PCI Express Models

Transceiver and Monitor

pcie_txrx_vmt, pcie_monitor_vmt Models

Overview

- PCI Express is a high-speed, serial interface replacement for the older PCI and PCI-X parallel bus standards
- The transceiver is fully bus functional, and can verify PCI Express endpoints, switches, and root complex devices
- The monitor provides detailed transaction logging and coverage of the PCI Express Compliance Checklist

Major Features

- Verification at PHY/MAC interface of x1, x2, x4, x8, x12, x16 lanes
- Supports Gen2 features and data rates
- Full Link Training (LTSSM) support
- Protocol and compliance monitor, which generates transaction and symbol log files
- Full Requester and Completer functions
- Multiple transfers initiated concurrently
- Automatically generates flow control packets
- Automatically handles Transaction, Data Link, and Physical layer tasks
- Requester and Completer operate concurrently using independent command channels
- Power management support
- Supports VCS Native Testbench (NTB)
- Supports the Reference Verification Methodology (RVM)
- Support *Verification Methodology Manual* (VMM) for SystemVerilog
- Highly configurable: number of lanes, process rates for received packets and completion packets, transaction ordering rules, packet payload sizes, symbol times between transmissions of Ack Data Link layer packets, number of SKIP symbols in a SKIP ordered-set, time out parameters, etc.

Requester

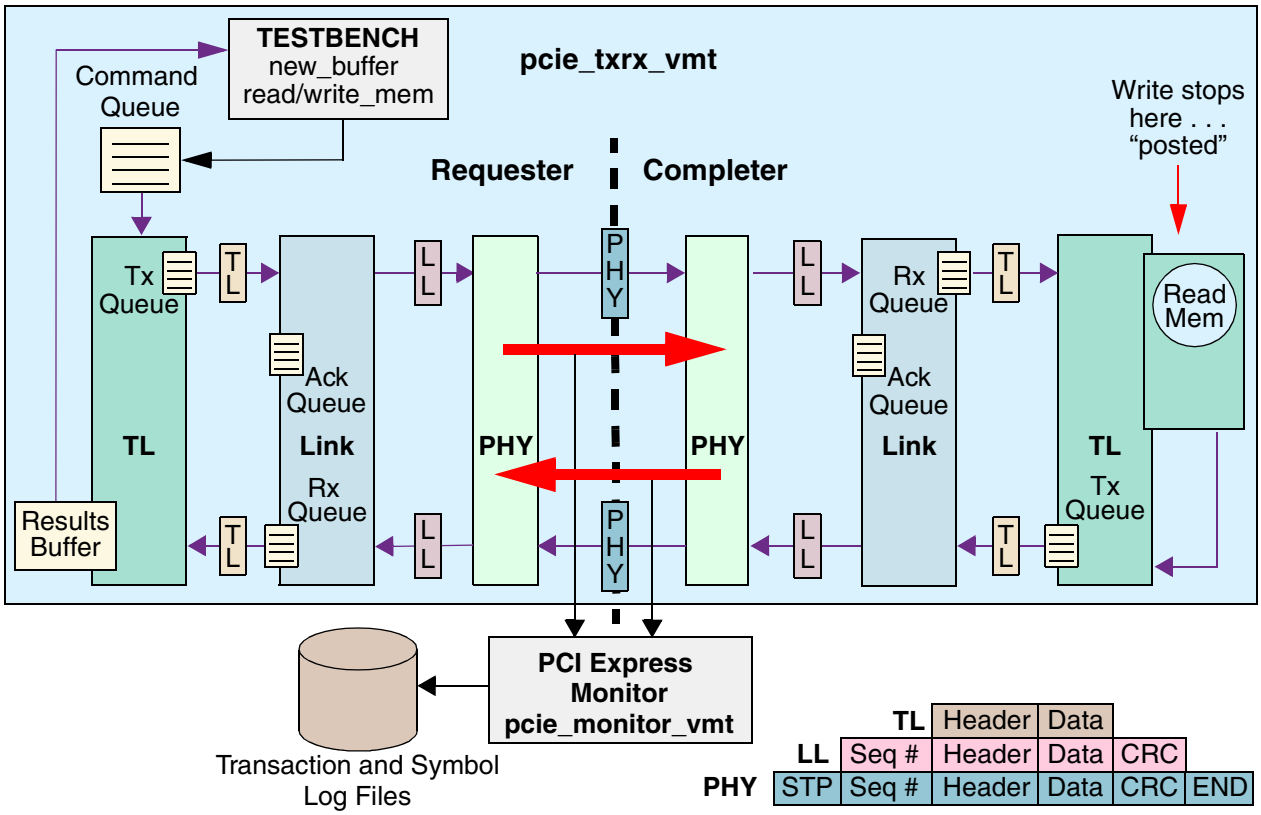
- Generates single word read and write transfers to memory, I/O, and configuration space
- Generates block read and write transfers to memory space
- Generates message transfers
- Transmits raw request packets created by user
- Custom error injection
- Automatic handling of completion packets, or optional handling of completion packets by testbench.

Completer

- Reads and writes internal address spaces in response to link requests
- Allows modification and review of internal address spaces with zero cycle commands
- Allows configuration of address ranges for internal memory and I/O spaces
- Returns raw request packets
- Transmits raw completion packets
- Creates completion packets for incoming requests
- Notifies testbench of significant events

Monitor

- Provides coverage of PCI Express compliance checklist. Coverage reports show checks passed, checks failed and checks not hit
- Logging of PCI Express transactions. Configurable to show start time, stop time, direction, packet type, sequence, credits and many other packet attributes.
- Records coverage for TLP types



The *DesignWare PCI Express Verification IP Databook* is available at:
http://www.synopsys.com/products/designware/docs

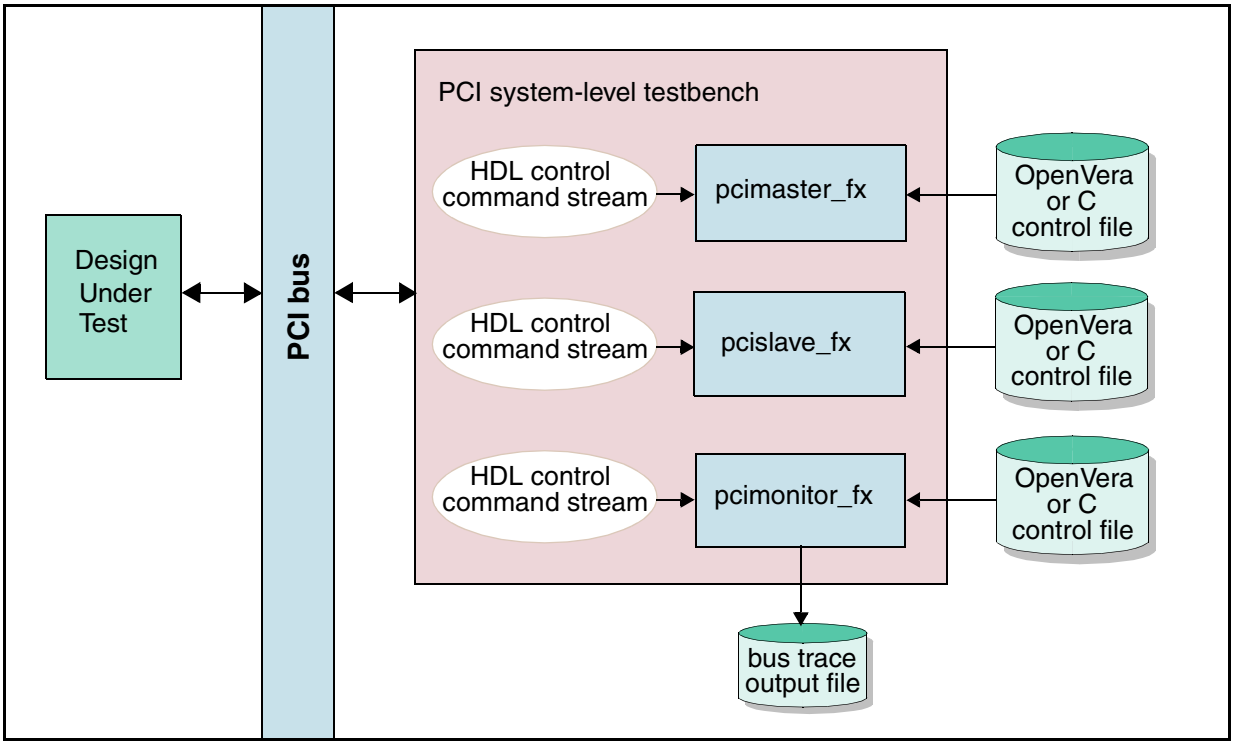
PCI / PCI-X Bus Models

Master, Slave, and Monitor

Overview

The Synopsys PCI/PCI-X FlexModel set consists of three separate PCI/PCI-X FlexModels and a set of system-level testbenches. The models support the PCI 2.3 and the PCI-X 1.0 and 2.0 specifications.

- **pcimaster_fx.** Performs timing violation checks and emulates the protocol of PCI/PCI-X initiators at the pin and bus-cycle levels. Initiates read and write cycles. In PCI-X mode, pcimaster_fx can function as a target for split transactions.
- **pcislave_fx.** Responds to cycles initiated by the pcimaster_fx model or by the user's PCI master device. In PCI-X mode, the pcislave_fx also functions as an initiator for split transactions.
- **pcimonitor_fx.** Monitors, logs, and arbitrates activity on the PCI or PCI-X bus.
- **PCI and PCI-X system testbenches.** Provides ready-to-use example testbenches for both conventional PCI mode and PCI-X mode. Each system testbench uses two pcimaster_fx models, two pcislave_fx models, and a pcimonitor_fx model.



The individual DesignWare FlexModel databooks are available with each model at:

http://www.synopsys.com/products/designware/ipdir

Serial ATA Models

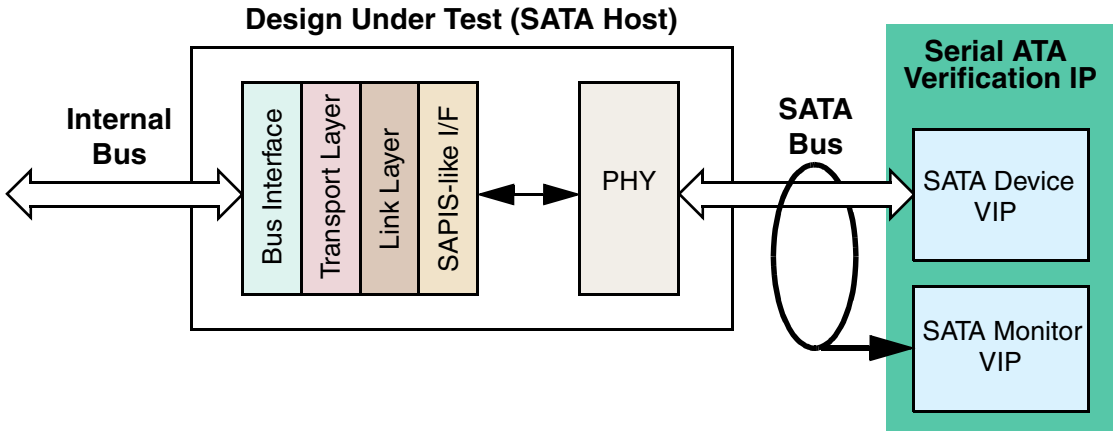
Device and Monitor

Device (sata_device_vmt)

- Gen 1 and Gen 2 support
- SATA PHY Interface (Differential NRZ serial stream)
- Transfer support includes:
  - PIO
  - First party DMA
  - Legacy and Legacy Queued DMA
  - Non-Data and PACKET command transfers
- Power-on sequencing and speed negotiation
- CRC computation, 8B/10B encoding and decoding, Scrambling/ Descrambling
- Native command queuing
- Power management
- Far-end retimed loop back, Far-end transmit only, and Far-end analog loop back BIST modes
- OOB signal detection and transmission
- Error injection/detection
- Supports VCS Native Testbench (NTB)
- Supports OpenVera Reference Verification Methodology (RVM).
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog

Monitor (sata_monitor_vmt)

- Gen 1 and Gen 2 support
- Snoops bus information
- Protocol coverage
- Checks the validity of the following aspects for the corresponding layers:
  - ***Physical*** -- Serialization/ Deserialization (SERDES), Out-of-band signaling
  - ***Link*** -- Framing, CRC, 8B/10B encoding, scrambling, running disparity
  - ***Transport*** -- FIS sequencing
  - ***Command*** -- Legacy DMA, Legacy queued DMA, Packet, PIO, Register and First-party DMA commands
- Native command queuing
- Issues informative messages
- Supports VCS Native Testbench (NTB)
- Supports OpenVera Reference Verification Methodology (RVM).
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog



The *DesignWare SATA Verification IP User Manual* is available at:
http://www.synopsys.com/products/designware/docs

Serial Input/Output Interface Models

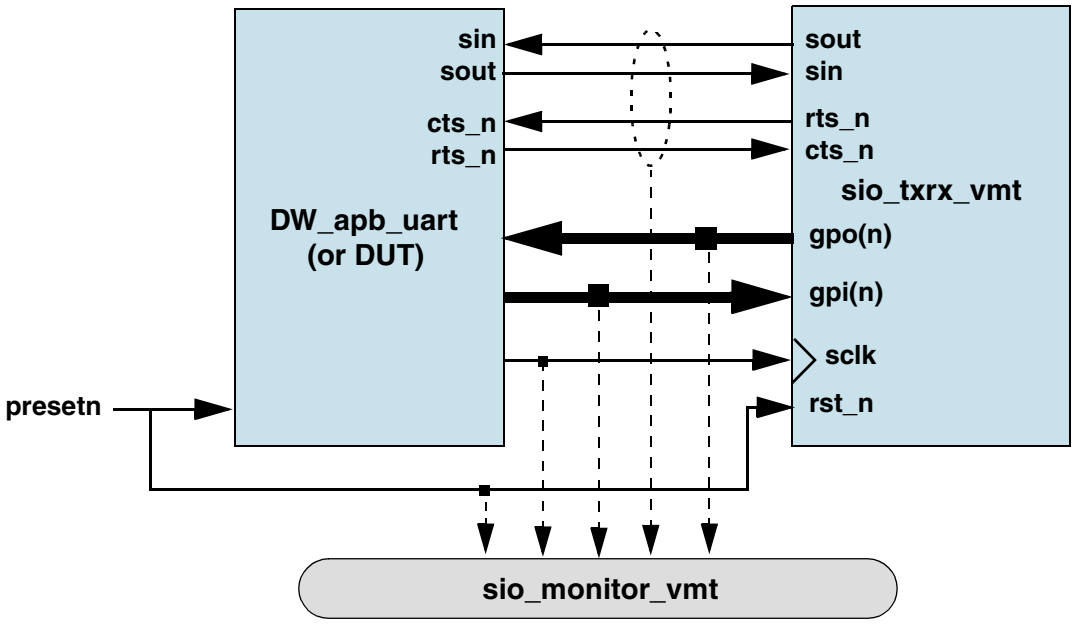
Tranceiver and Monitor

SIO TxRx Model (sio_txrx_vmt)

- Full duplex operation
- Fully configurable serial interface
- Both GPIO and SIO port interfaces
- Configurable receive FIFO depth
- Configurable internal baud clock
- Programmable hardware flow control
- IrDA SIR (infrared) mode support
- Error generation/injection capability
- Parity generate/check (odd/even/none/space/mark)
- Robust command set control
- Supports VCS Native Testbench (NTB)
- Supports OpenVera Reference Verification Methodology (RVM)
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog

SIO Monitor Model (sio_monitor_vmt)

- Protocol checking
- Transaction logging
- Watchpoint monitoring
- Configurable to match TxRx model
- Configurable internal baud clock
- Programmable hardware flow control
- IrDA SIR (infrared) mode support
- Parity generation and checking
- Command set control
- Supports VCS Native Testbench (NTB)
- Supports OpenVera Reference Verification Methodology (RVM)
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog



The *DesignWare SIO Verification IP Databook* is available at:
http://www.synopsys.com/products/designware/docs

USB On-The-Go Models

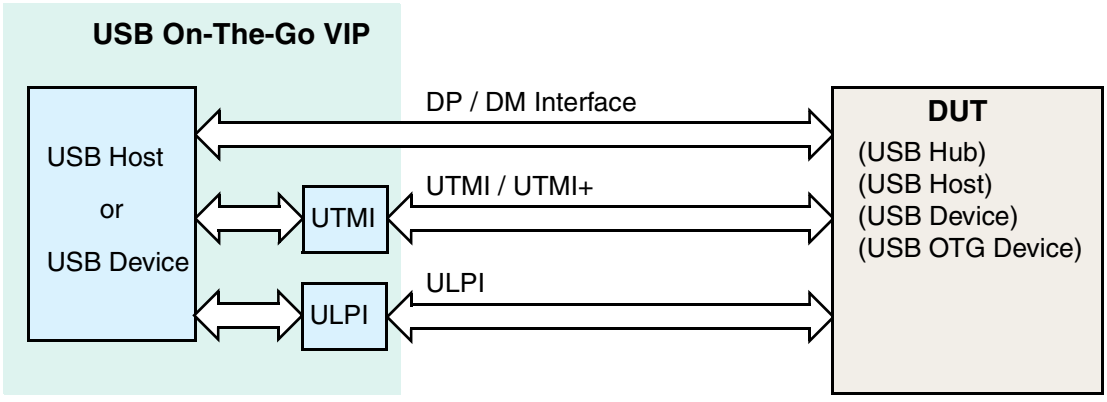
Host and Device

USB Host Model (usb_host_vmt)

- 1.1, 2.0, OTG, UTMI+, ULPI, HSIC, and IC_USB
- High, full, and low speeds
- Operation at packet and transaction levels
- USB signaling with programmable timers
- Suspend, resume, reset signaling
- Link Power Management (LPM)
- Error generation capabilities
- Programmable inter-packet and end-to-end delays
- Supports VCS Native Testbench (NTB)
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog and OpenVera (RVM)

USB Device Model (usb_device_vmt)

- 1.1, 2.0, OTG, UTMI+, ULPI, HSIC, and IC_USB
- Configures to Non-OTG, SRP Host only, SRP Peripheral only, Dual Role OTG A, Dual Role OTG B
- Operation at packet and transaction levels
- High, full, and low speeds
- Programmable response for endpoints
- Packet error injection/detection
- Suspend, resume, reset signaling
- Link Power Management (LPM)
- Supports SRP and HNP
- Supports VCS Native Testbench (NTB)
- Supports *Verification Methodology Manual* (VMM) for SystemVerilog and OpenVera (RVM)



A guide to all USB VIP documentation is available at:

https://www.synopsys.com/dw/doc.php/vip/usb/latest/doc/usb__overview.pdf

DesignWare FlexModels

FlexModels are binary simulation models that represent the bus functionality of microprocessors, cores, digital signal processors, and bus interfaces. FlexModels utilize the industry-standard SWIFT interface to communicate with simulators. FlexModels have the following features:

- Built with a cycle-accurate core and a controllable timing shell so that you can run the model in function-only mode for higher performance, or with timing mode enabled when you need to check delays. You can switch between timing modes dynamically during simulation using simple commands in your testbench.
- Feature multiple/different control mechanisms. You can coordinate model behavior with simulation events, synchronize different command processes, and control several FlexModels simultaneously using a single command stream.
- Allow you to use different command sources. You can send commands to DesignWare Librarys using processes in a Verilog or VHDL testbench, a C program, or a OpenVera testbench. You can switch between the HDL or OpenVera testbench and a compiled C program as the source for commands.

Listing of FlexModels

Table 1 lists the FlexModels that are available, including a brief description.

Table 1: Listing of FlexModels

Model Name	Vendor	Description
Bus Models		
enethub_fx	Ethernet	Emulates the protocol of Ethernet Hub at the pin and bus-cycle levels; handles data routing from TX to RX.
rmiis_fx	Ethernet	Interface between MII and reduced RMII interface.
pcimaster_fx	PCI/PCI-X	Emulates the protocol of PCI/PCI-X initiators at the pin and bus-cycle levels. Initiates read and write cycles.
pcislave_fx	PCI/PCI-X	Responds to cycles initiated by the pcimaster_fx model or by the user's PCI master device.
pcimonitor_fx	PCI/PCI-X	Monitors, logs, and arbitrates activity on the PCI or PCI-X bus.
Support Models		
sync8_fx	Synopsys	8-bit synchronization model

More information on these models is available from the following Web page:

http://www.synopsys.com/products/designware/dwverificationlibrary.html

The *FlexModel User's Manual* is available at:

http://www.synopsys.com/products/designware/docs

DesignWare SmartModels

The SmartModel Library is a collection of over 3,000 binary behavioral models of standard integrated circuits supporting more than 12,000 different devices. The library features models of devices from the world's leading semiconductor manufacturers, including microprocessors, controllers, peripherals, memories, and general-purpose logic. SmartModels connect to logic simulators through the SWIFT interface, which is integrated with over 30 commercial simulators, including Synopsys VCS and VCS MX, Cadence Verilog-XL, and Mentor Graphics QuickSim II.

Instead of simulating devices at the gate level, SmartModels represent integrated circuits and system buses as "black boxes" that accept input stimulus and respond with appropriate output behavior. Such behavioral models are distributed in object code form because they provide improved performance over gate-level models, while at the same time protecting the proprietary designs created by semiconductor vendors.

All SmartModels and model datasheets are listed in the IP Directory:

http://www.synopsys.com/dw/ipsearch.php

SmartModel Features

- Support for "Windows" allowing you to view and change internal register values.
- Consistent SWIFT interface across most simulators.
- Simulation-efficient behavorial-level models.
- Industry-standard as well as configurable timing behavior.

SmartModel Types

There are two basic types of SmartModels:

- Full-functional Models (FFMs) simulate the complete range of device behavior.
- Bus-Functional Models (BFMs) simulate all device bus cycles. FlexModels are a type of BFM in the SmartModel Library, which you can control using Verilog, VHDL, OpenVera, or C.

For some devices, more than one type of model may be available, but these are exceptions, not the general rule. For detailed information about a specific SmartModel (including FlexModels), refer to the model's datasheet. For an overview of the FlexModels, see "DesignWare FlexModels" on page 96.

SmartModel Timing Definitions

All SmartModels have at least one timing version. To see what timing versions are available for a particular model, use the Browser tool to display a list of timing versions for that model.

If you need a timing version that is not supplied with the library, or if you want to back-annotate customized delays into the model's simulation, you can create a custom timing version as described in "User-Defined Timing" in the *Smartmodel Library User's Manual*.

Specific Model Information

SmartModel datasheets provide specific user information about each model in the library. The model datasheets supplement, but do not duplicate, the manufacturer's datasheets for the hardware parts. In general, the model datasheets describe:

- Supported hardware IP and devices
- Bibliographic sources used to develop the model (specific vendor databooks or datasheets)
- How to configure and operate the model
- Any timing parameters that differ from the vendor specifications
- How to program the device (if applicable) or otherwise use it in simulation
- Differences between the model and the corresponding hardware device

Models are partitioned by function, including:

- Processors/VLSI
- Programmables
- Memories
- Standards/Buses
- General Purpose

SmartModel datasheets have standard sections that apply to all models and model-specific sections whose contents depend on the model type.

3 DesignWare Foundry Libraries

This chapter briefly describes the DesignWare Foundry Libraries. Synopsys is teaming with foundry leaders to provide DesignWare Library licensees access to standard cells memories and I/Os optimized for their process technologies. Each library is delivered in a set of front-end and back-end views. The front-end views enable a complete evaluation of the libraries, all the way through layout and complete verification. The back-end views include the GDSII data and tech files necessary for tape-out.

TSMC Libraries

TSMC and Synopsys offer a complete path from RTL to GDSII by ensuring a tight integration of the TSMC Libraries and the Synopsys Galaxy platform through the TSMC Reference Flow 8.0. Both the front-end and back-end views of the TSMC 0.15, 0.13 micron, Nexsys 90 nanometer, and Nexsys 65 nanometer Standard Cells and I/Os are available to DesignWare Library licensees at no additional cost. A selection of memory compilers for TSMC Nexsys 90LP and TSMC Nexsys 65LP process (described on page 105) are also available and licensed independently from the DesignWare Library.

TSMC Libraries are developed by TSMC and process-tuned to TSMC's semiconductor technologies. Each logic and I/O cell is validated in silicon and meets the company's rigorous library quality criteria. TSMC libraries are in production in multiple customer designs.

Table 1 on page 101 shows the TSMC Standard I/O categories. Table 2 on page 102 shows the TSMC Standard Cell categories.

For more information about the TSMC Libraries, visit http://www.synopsys.com/products/designware/tsmc.html

Table 1: TSMC Standard I/O Categories

Technology	Process	Core Voltage	I/O Voltage	Configuration	Library Name
65nm	Low Power	1.2V All	2.5V; 3.3V tol.	Staggered Universal	TPZN65LPGV2
			All	Staggered Universal	TPBN65GV
90nm	General Purpose	1.0V	2.5V	Staggered	TPDN90G2
			1.8V	Staggered	TPDN90G18
			3.3V	Staggered	TPDN90G3
130nm	General Purpose	1.2V-HVT	2.5V; 3.3V tol.	Staggered	TPZ013G2
			3.3V; 5V tol.	Staggered	TPZ013G3
		1.2V	2.5V	Linear	TPD013N2
			3.3V	Linear	TPD013N3
	Low Voltage	1.0V-HVT	2.5V; 3.3V tol.	Staggered	TPZ013LG2
		1.0V-OD	2.5V; 3.3V tol.	Staggered	TPZ013LODG2
		1.0V-HVT	3.3V; 5V tol.	Staggered Universal	TPZ013LGV3
		1.0V-OD	3.3V; 5V tol.	Staggered Universal	TPZ013LODGV3
		All	All	Staggered Universal Pads	TPB013GV
	Low Power	1.5V	2.5V	Linear	TPD013LPN2
			3.3V	Linear	TPD013LPN3
150nm	General Purpose	1.5V	3.3V; 5V tol.	Staggered	TPZ015G
	Low Voltage	1.2V	3.3V; 5V tol.	Staggered	TPZ015LG

Table 2: TSMC Standard Cell Categories

Tech	Process	Feature	Library Name
65nm	G Plus	Nominal VT	TCBN65GPLUS
		Low VT	TCBN65GPLUSLVT
		High VT	TCBN65GPLUSHVT
		Nominal VT with MTCMOS support	TCBN65GPLUSCG
		Low VT with MTCMOS support	TCBN65GPLUSCGLVT
		High VT with MTCMOS support	TCBN65GPLUSCGHVT
	Low Power (LP)	Nominal VT	TCBN65LP
		Low VT	TCBN65LPLVT
		High VT	TCBN65LPHVT
		Nominal VT with MTCMOS support	TCBN65LPCG
		Low VT with MTCMOS support	TCBN65LPLVTCG
		High VT with MTCMOS support	TCBN65LPHVTCG

Table 2: TSMC Standard Cell Categories (Continued)

Tech	Process	Feature	Library Name
90nm	General Purpose (G)	Nominal VT with Multi-VDD support	TCBN90GHP
		Low VT with Multi-VDD support	TCBN90GHPLVT
		High VT with Multi-VDD support	TCBN90GHPHVT
		Nominal VT with MTCMOS support	TCBN90GHPCG
		Low VT with MTCMOS support	TCBN90GHPCGLVT
		High VT with MTCMOS support	TCBN90GHPCGHVT
		Nominal VT with Back Bias support	TCBN90GHPWB
		Low VT with Back Bias support	TCBN90GHPLVTWB
		High VT with Back Bias support	TCBN90GHPHVTWB
		Overdrive - Nominal VT	TCBN90GHPOD
		Overdrive - Low VT	TCBN90GHPODLVT
		Overdrive - High VT	TCBN90GHPODHVT
	High Performance (GT)	Nominal VT	TCBN90GTHP
		Low VT	TCBN90GTHPLVT
		High VT	TCBN90GTHPHVT
	Low Power (LP)	Nominal VT with Multi-VDD support	TCBN90LPHP
		Low VT with Multi-VDD support	TCBN90LPHPLVT
		High VT with Multi-VDD support	TCBN90LPHPHVT
		Ultra High VT	TCBN90LPHPUHVT
		Nominal VT with Back Bias support	TCBN90LPHPWB
		Low VT with Back Bias support	TCBN90LPHPLVTWB
		High VT with Back Bias support	TCBN90LPHPHVTWB
		Nominal VT with MTCMOS support	TCBN90LPHPCG
		Low VT with MTCMOS support	TCBN90LPHPLVTCG
		High VT with MTCMOS support	TCBN90LPHPHVTCG

Table 2: TSMC Standard Cell Categories (Continued)

Tech	Process	Feature	Library Name
130nm	General Purpose	Nominal VT	TCB013GHP
		Low VT	TCB013GHPLVT
		High VT	TCB013GHPHVT
	Low Voltage	Nominal VT	TCB013LVHP
		High VT	TCB013LVHPHVT
		Over Drive 1.2V	TCB013LVHPOD
		Over Drive 1.2V, High VT	TCB013LVHPODHVT
	Low Power	Nominal VT	TCB013LPHP
		Low VT	TCB013LPHPLVT
150nm	General Purpose	Nominal VT	TCB015GHD
	Low Voltage	Nominal VT	TCB015LVHD

TSMC Memory Compilers for 90LP and 65LP

Table 3 shows TSMC Nexsys Memory Compilers for 65LP technology.

Table 3: TSMC 65LP compilers

Description	Features
Single Port SRAM With Redundancy	1K~256K
Single Port SRAM W/o Redundancy	64~256K
Dual Port SRAM	64~1152K
1 Port Register File	16~18K
2 Port Register File	16~72K
ROM	64~1152K
Single Port SRAM W/o Redundancy - HVT	64~256K; Low Leakage
Dual Port SRAM - HVT	64~1152K; Low Leakage
1 Port Register File - HVT	16~18K ; Low Leakage
2 Port Register File - HVT	16~72K; Low Leakage
ROM - HVT	64~1152K ; Low Leakage

Table 4 shows TSMC Nexsys Memory Compilers for 90LP technology.

Table 4: TSMC 90LP compilers

Description	Features
Single Port SRAM With Redundancy - HD	64~512Kbits; 0.999um2 bitcell
Single Port SRAM W/o Redundancy – HD; HVT	64~512Kbits; 0.999um2 bitcell
Dual Port SRAM	64~256Kbits
Dual Port SRAM - HVT	64~256Kbits; Low Leakage
2 Port Register File	32~32Kbits
2 Port Register File with Redundancy	64~256Kbits
2 Port Register File - HVT	32~32Kbits; Low Leakage
ROM	1K~2Mbits
ROM - HVT	1K~2Mbits; Low Leakage

Chartered Libraries

Synopsys and Chartered Semiconductor have partnered to develop, license, and distribute a complete offering of high performance standard cells, I/Os, and memory compilers optimized for Chartered's 0.35um, 0.25um, 0.18um, and 0.13um process offerings. Based on Synopsys library development technology and methodology, the Chartered libraries are a set of technology-aggressive, high-performance, and high-density foundation intellectual property (IP) specifically targeted for manufacture of IC designs at Chartered Semiconductor. Table 5 lists the library components, which includes standard cells, I/Os, and memory compilers. All are optimized to Chartered's process design rules. The libraries have been silicon tested to validate maximum performance and reliability. The libraries support an open electronic design automation (EDA) environment.

The Chartered Libraries distributed through DesignWare are an ideal solution for both all-digital integrated circuit and mixed-signal designs.

Table 5: Chartered Libraries

Tech	Library	Description	Name
0.13µm	Standard Cells	Logic	chrt13fs122
	I/Os	Inline - 1.2/2.5V 3.3V tolerant	chrt13io222
		Inline - 1.2/3.3V 5V tolerant	chrt13io322
		Staggered - 1.2/2.5V 3.3V tolerant	chrt13sio222
		Staggered - 1.2/3.3V 5V tolerant	chrt13sio322
		Inline PCI 133MHz I/Os 1.2/3.3V	chrt13pc322
		Staggered PCI 133MHz I/Os 1.2/3.3V	chrt13spc322
	RAM Compilers	High Density synchronous single-port	chrt13rs162
		Synchronous dual-port	chrt13rd142
		Asynchronous two-port	chrt13rt162
	ROM Compiler	Synchronous, diffusion programmable	chrt13ro152

Table 5: Chartered Libraries (Continued)

Tech	Library	Description	Name
0.18 µm	Standard Cells	Logic	csm18os120
	I/Os	In line - 1.8/3.3V 5V tolerant	csm18io221
		Staggered - 1.8/3.3V 5V tolerant	csm18sio221
		In line PCI I/Os 1.8/3.3V 5V tolerant	csm18pc220
		Staggered PCI I/Os 1.8/3.3V 5V tolerant	csm18spc220
	RAM Compilers	Single port HD synchronous	csm18rs161
		Dual port synchronous	csm18rd131
		Two-port asynchronous	csm18rt151
	ROM Compiler	Synchronous, diffusion programmable	csm18ro151
0.25 µm	Standard Cells	Logic	csm25os163
	I/Os	In line - 3.3V 5V tolerant	csm25io223
		Staggered - 3.3V 5V tolerant	csm25sio223
		In line PCI - 3.3V 5V tolerant	csm25pc223
		Staggered PCI - 3.3V 5V tolerant	csm25spc223
	RAM Compilers	Single port synchronous	csm25rs144
		Single port HD synchronous	csm25rs160
		Dual port asynchronous	csm25rd114
		Two-port asynchronous	csm25rt134
		Single-port asynchronous	csm25ra114
	ROM Compiler	Synchronous, diffusion programmable	csm25ro144
0.35 µm	Standard Cells	Logic	csm35os142
	I/Os	In line - 3.3V 5V tolerant	csm35io122
		In line PCI 3.3V 5V tolerant	csm35pc132
	RAM Compilers	Single port synchronous	csm35rs142
		Single port asynchronous	csm35ra112
		Dual port asynchronous	csm35rd112
		Two-port asynchronous	csm35ra122
	ROM Compiler	Synchronous, diffusion programmable	csm35ro122

4 DesignWare Cores (Digital and Mixed-Signal IP)

DesignWare Cores provide system designers with silicon-proven, digital and analog connectivity IP. Provided as heavily-annotated, synthesizable RTL source code, or in GDS format, these cores enable you to design innovative, cost-effective systems-on-chip and embedded systems. DesignWare Cores are licensed individually on a fee-per-project business model. The following table identifies the DesignWare Cores offering:

Component Name	Component Description	Component Type
Ethernet Cores		
dwc_ethernet_mac10_100_universal	Ethernet MAC 10/100 Universal (page 111)	Synthesizable RTL
dwc_ether_mac10_100_1000_universal	Ethernet MAC 10/100/1G Universal (page 113)	Synthesizable RTL
dwc_ether_xgmac	10 Gigabit Ethernet Mac (page 115)	Synthesizable RTL
dwc_ethernet_pcs	PCS Layer of 10 Gigabit Extended sub-layer (page 117)	Synthesizable RTL
dwc_xaui_phy	XAUI PHY (page 174)	Hard IP
Mobile Storage Core		
dwc_mobile_storage	Secure Digital (SD), Multimedia Card (MMC) and CE-ATA (page 119)	Synthesizable RTL
DDR*n* SDRAM Core		
DDR2/3-Lite SDRAM Complete Solution	High performance DDR2/3 SDRAM interfaces up to 1066 Mbps (page 125)	Synthesizable RTL and Hard IP

DDR2/DDR SDRAM PHY and Controller	DDR2/DDR SDRAM Complete Solution (page 127)	Synthesizable RTL and Hard IP
IEEE 1394 Cores		
dwc_1394_av_link	IEEE 1394 AVLink (page 121)	Synthesizable RTL
dwc_1394_cphy-native	IEEE 1394 Cable PHY (page 123)	Synthesizable RTL
JPEG Core		
dwc_jpeg	JPEG CODEC (page 129)	Synthesizable RTL
PCI Cores		
dwc_pci	32/64 bit, 33/66-MHz PCI Core (page 131)	Synthesizable RTL
dwc_pci-x	32/64 bit, 133-MHz PCI-X Core (page 133)	Synthesizable RTL
PCI Express Cores		
dwc_pci_express_ep	PCI Express Endpoint Core (page 138)	Synthesizable RTL
dwc_pci_express_rc	PCI Express Root Port Core (page 140)	Synthesizable RTL
dwc_pci_express_sw	PCI Express Switch Port Core (page 142)	Synthesizable RTL
dwc_pci_express_dm	PCI Express Dual Mode Core (page 144)	Synthesizable RTL
dwcore_pcie_phy	PCI Express PHY Core (page 146)	Hard IP
SATA Cores		
dwc_sata_ahci	SATA AHCI (page 148)	Synthesizable RTL
DWC_dsata	SATA Device (page 150)	Synthesizable RTL
dwc_sata_phy	SATA PHY (page 152)	Hard IP

USB Cores		
dwc_usb_1_1_device	USB 1.1. Device Controller (page 154)	Synthesizable RTL
dwc_usb_1_1_ohci_host	USB 1.1 OHCI Host Controller (page 156)	Synthesizable RTL
dwc_usb_1_1_hub-native	USB 1.1. Hub Controller (page 158)	Synthesizable RTL
dwc_usb_2_0_host_subsystem-pci-ahb	USB 2.0 Host Controller - UHOST2 (page 160)	Synthesizable RTL
dwc_usb_2_0_hs_otg_subsystem-ahb	USB 2.0 Hi-Speed On-the-Go Controller Subsystem (page 162)	Synthesizable RTL
dwc_usb_2_0_device	USB 2.0 Device Controller (page 164)	Synthesizable RTL
dwc_usb2_phy	USB 2.0 PHY (page 166)	Hard IP
dwc_usb2_hsotg_phy	USB 2.0 Hi-Speed On-the-Go PHY (page 168)	Hard IP
dwc_wiusb_device_controller	Wireless USB Device Controller (page 170)	Synthesizable RTL
dwc_usb2_nanophy	USB 2.0 nanoPHY (page 172)	Hard IP

dwc_ethernet_mac10_100_universal

Ethernet MAC 10/100 Universal Core

The DesignWare Ethernet MAC 10/100 Universal Core enables the host to communicate data using the Ethernet protocol (IEEE 802.3). This silicon-proven core is configurable and scalable to meet multiple Ethernet application requirements and system architectures. Its high-performance architecture is optimized for low latency and low gate count.

The Synopsys Ethernet MAC 10/100 Universal Core enables Ethernet functionality for switch, NIC, and system-on-chip applications. The DesignWare Ethernet MAC implements more functionality than standard Ethernet MACs, including MAC station management, address check, IP checksum offload engine, time stamping and Control/ Status Register (CSR) blocks. These additional features provide higher-level system functionality usually implemented in firmware or using separate products. With these additional capabilities, the Ethernet MAC simplifies system implementation.

General Features

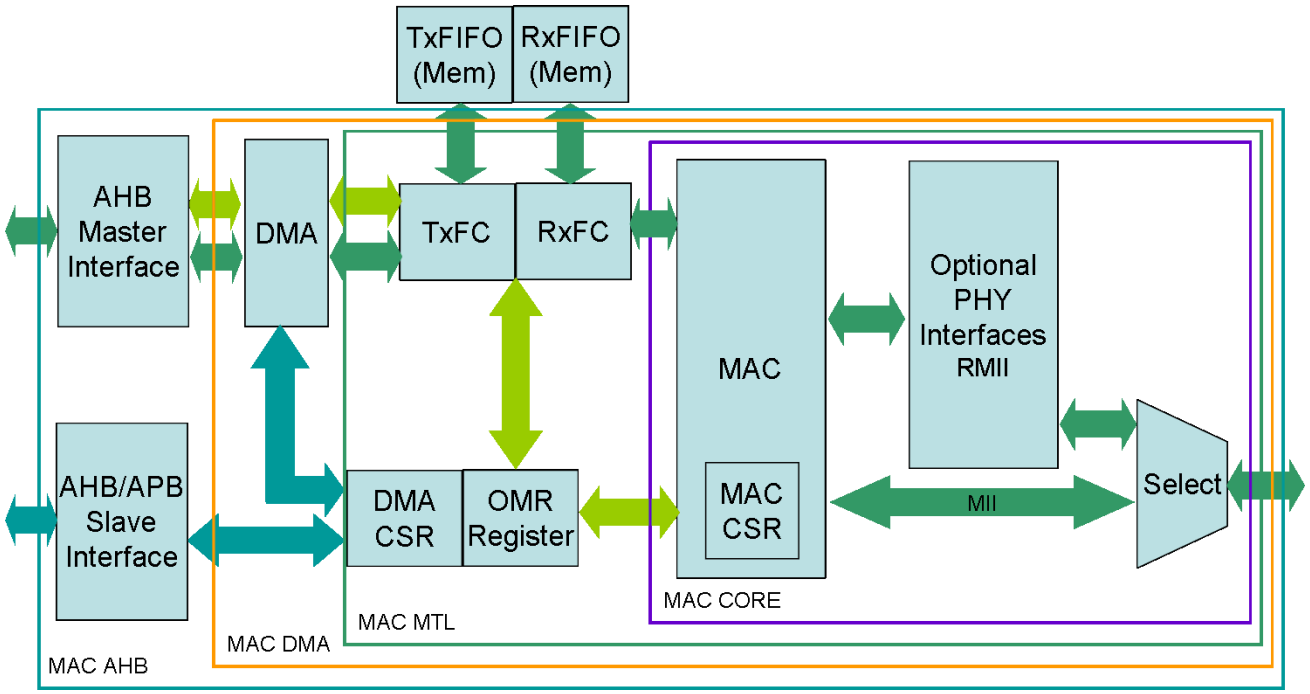
- Complies with the full IEEE 802.3-2002 specification.
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Supports CSMA/CD protocol for half duplex operation
- Supports Full Duplex Only configuration
- Supports IEEE 802.3x flow control for full duplex operation
- Supports IEEE 1588-2002 precision clock synchronization
- Optional module for LAN wakeup frames and AMD Magic Packet frames

PHY Interface Features

- Supports SMII/MII/RMII interfaces
- MDIO Master Interface (optional) for PHY device configuration and management

Application Interface Features

- Data interface configurable to support FIFO interface or AHB interface
- CSR interface configurable to AHBTM Slave or APBTM Slave (32-bit) interface
- Supports 32/64/128-bit data on the AHB master and slave ports
- Supports SPLIT, RETRY, and ERROR AHB responses in AHB master interface
- Configurable for little- or big-endian modes
- Supports all AHB burst types in AHB slave interface
- Software can select the type of AHB burst in an AHB master interface
- Receive checksum offload for IP, TCP/UDP packets



The dwc_ethernet_mac10_100_universal datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_ether_mac10_100_universal.pdf

dwc_ether_mac10_100_1000_universal

Ethernet MAC 10/100/1000 Universal Core

The Synopsys DesignWare Ethernet MAC 10/100/1G Universal Core enables the host to communicate using the Gigabit Ethernet protocol (IEEE 802.3). The Ethernet MAC 10/100/1G Universal Core is composed of three main layers: the Gigabit Ethernet Media Access Controller (GMAC), the MAC Transaction Layer (MTL), and the MAC DMA Controller (MDC). Other features include the following:

General Features

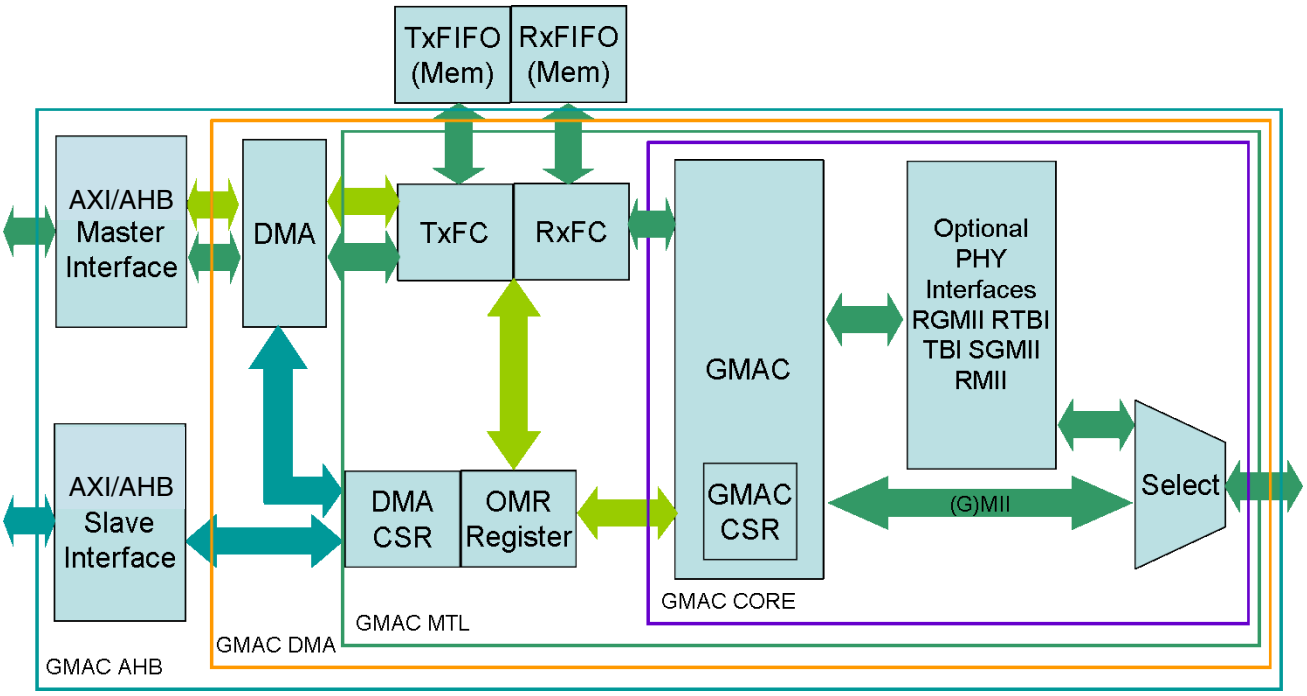
- Compliant with IEEE 1588-2002 and IEEE 1588-2008 Precision Clock Synchronization
- Complies with the full IEEE 802.3-2002 specification.
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Configurable to support the following data transfer rates:
  - 10-, 100-, or 1000-Mbps
  - 10 or 100 Mpbs only
  - 1000 Mbps only
- Supports CSMA/CD protocol for half duplex operation
- Supports Full Duplex Only configuration
- Supports packet bursting and frame extension in 1000-Mbps Half Duplex mode
- Supports IEEE 802.3x flow control for full duplex operation
- Supports a variety of flexible address filtering modes
- Complete network statistics (optional) with RMON/MIB counters (RFC2819/RFC2665)

PHY Interface Features

- IEEE 802.3-compliant GMII/RGMII MII/RMII
- IEEE 802.3z-compliant TBI/RTBI with auto-negotiation support
- Supports SGMII
- Supports Serial-MII (SMII)
- MDIO Master interface (optional) for PHY device configuration and management

Application Interface Features

- The following application interfaces are configurable:
  - GMAC-only with native interface
  - GMAC with MTL native interface
  - DMA with native interface
  - DMA with AHB interface
  - DMA with AXI interface
- Data interface, configurable to support FIFO or AHB interfaces
- CSR interface, configurable to AHB Slave or APB Slave (32-bit) interface
- Supports 32-, 64-, or 128-bit data on the AHB Master port



The dwc_ethernet_mac10_100_1G_universal datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_ether_mac10_100_1000_universal.pdf

dwc_ether_xgmac

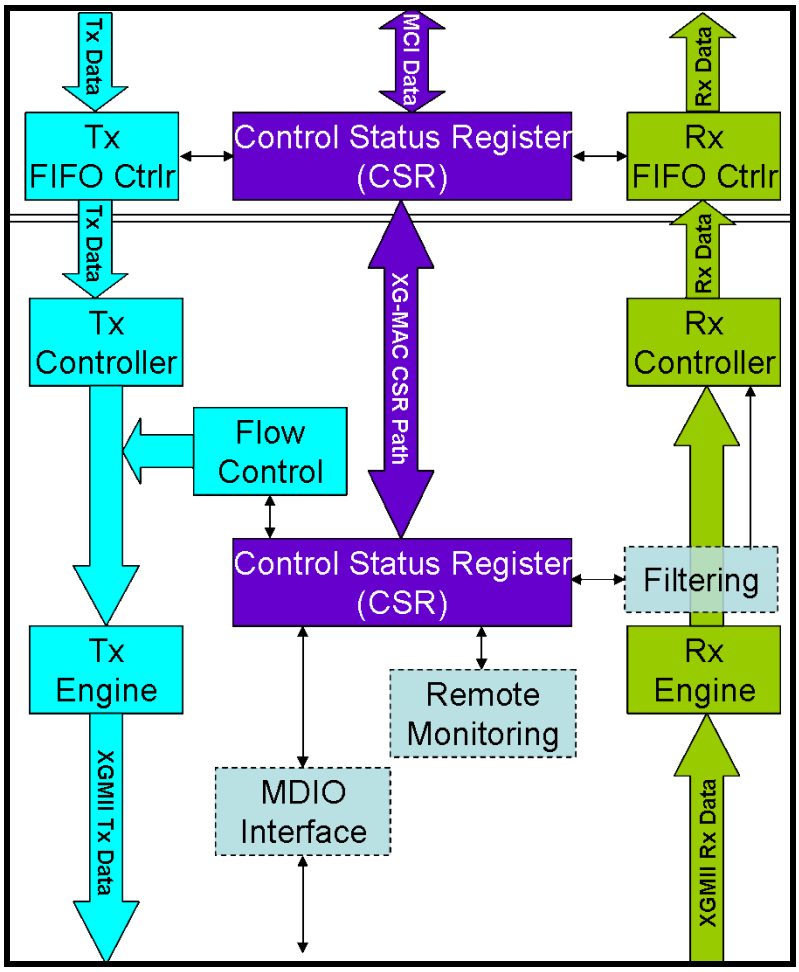
XGMAC 10G Ethernet MAC

The DesignWare XGMAC core is specifically designed for easy integration with 1G/ 2.5G/10G-Ethernet host applications. The XGMAC core has a simple FIFO interface on the transmit and receive sides for transferring data to the application. The generic interface provides simple controls for the data transfer and extraction of FIFO status information. This enables the host application to access the XGMAC's control and status registers (CSRs), thus giving the host CPU easy access to the native 32-bit read/write bus.

The XGMAC subsystem provides a 10-Gigabit Media-Independent Interface (XGMII, an IEEE 802.3ae compliant reconciliation sub-layer) for communication with the 10-Gigabit PHY. The XGMAC IP also provides a Management Data Input/Output (MDIO) interface capable of addressing MDIO devices that comply with Clause 45 of the IEEE 802.3ae standard and Clause 22 of the 802.3-2005 standards.

Features

- IEEE 802.3ae XGMII
- IEEE 802.3ae 31-bit flow control
- IEEE 802.3-2005 Clause 35 GMII Interface
- IEEE 802.3x Flow Control for full duplex operation
- IEEE 802.1Q VLAN receive tag detection
- Support for VLAN tag inclusion/replacement/detection on transmit.
- Separate transmission, reception and control interfaces.
- Optional forwarding of received pause control frames.
- Automatic transmission of zero-quanta pause frame on flow-control input deassertion.
- 32-bit CRC generation for transmit frames
- Per-frame CRC checking and stripping on receive
- Transmission and receive padding enabled for less than 64 bits
- Jumbo Ethernet frame support up to 64KB
- 64-bit status returned for each transmitted or received packet
- Programmable address inclusion/replacement for transmit frames
- IPv4 header checksum procession for transmit and receive
- Optional Network statistics with ROM/MIB counters
- Optional internal loop-back on XGMII for system packet debugging
- Configurable filtering, transition layer, Tx/Rx FIFO and debugging support.
- TCP, UDP, or ICMP checksum offload (IPv4 and IPv6) for transmission and reception



The dwc_ether_xgmac datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_ether_xgmac.pdf

dwc_ethernet_pcs

Ethernet Extension Sub-layer

The DesignWare Ethernet PCS Core complies with the IEEE 802.3ae specifications, Clause 47 and Clause 48 for XGXS applications, and complies with the IEEE 802.3ap specification, Clause 36, Clause 45, Clause 48 and Clause 73 for supporting 1000B-KX, 10GBASE-KX4, and auto-negotiation. The core is verified using state-of-the-art methodologies to reduce risk. This includes RTL design, verification, hardware verification and interoperability tests.

The Ethernet PCS is easily configured with a user friendly application interface, which enables you to achieve functional and implementation objectives to meet design requirements, such as datapath width and operating frequency. Using the Ethernet PCS core with the DesignWare Cores XG-MAC, a configurable Media Access Control (MAC) core that supports 1-, 2.5- and 10-Gigabit Ethernet applications, and with the DesignWare XAUI-PHY, a complete XAUI solution for 10-Gigabit Ethernet, enables easy SoC integration into a 10-Gigabit design.

General Features

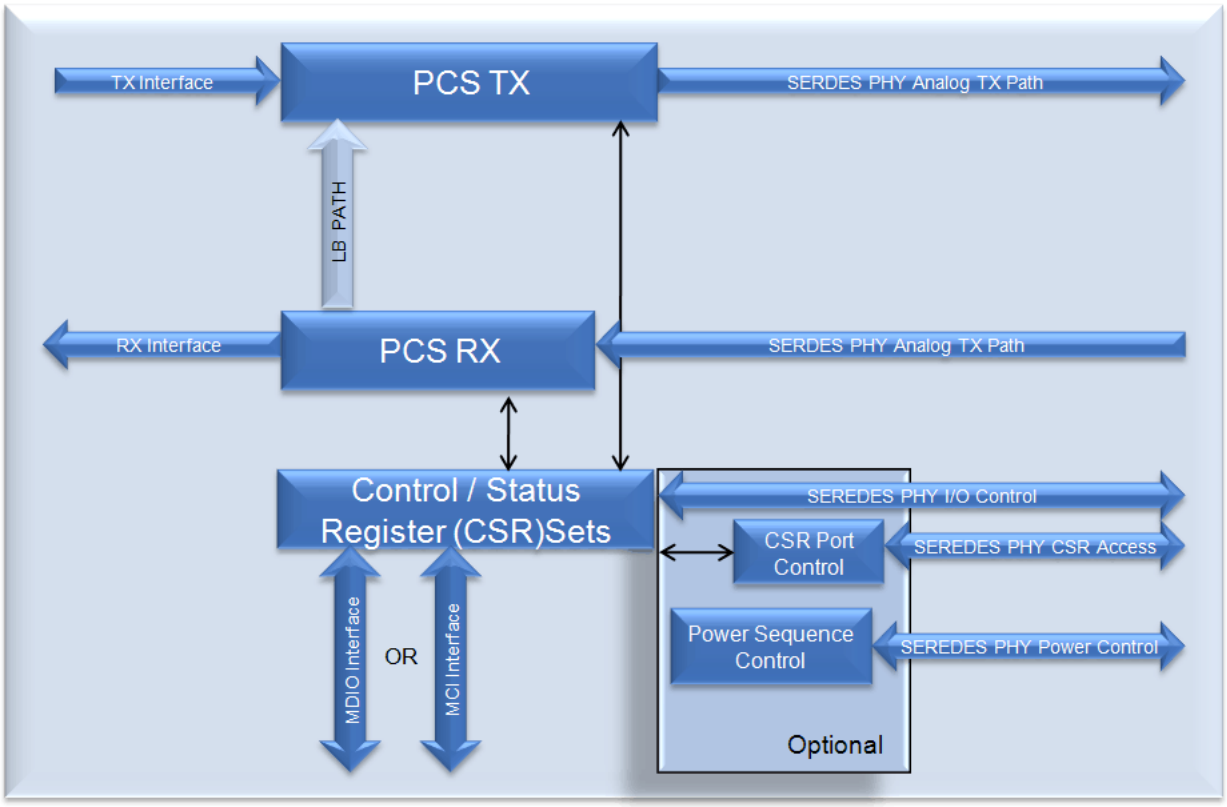
- Compliant with IEEE 802.3ae Clauses 47 and 48 for XGXS applications and IEEE 802.3ap Clauses 36, 45, 48 and 73 for 1000B-KX, 10GBASE-KX4, and auto-negotiation
- Backplane Ethernet for KX and KX4, KX only or KX4 only with KX configurations capable of 2.5 Gigabit Ethernet speeds simply by a clock frequency increase

Transmit Path

- Conversion of dual data rate XGMII to single data rate 312.5 MHz data bus
- Optional conversion of double data-width (64-bit) XGMII operating with 156.25 MHz clock to single data rate (32-bit) operation with a 312.5 MHz clock
- Conversion of XGMII idle control characters to a randomized sequence of code groups to enable lane synchronization, lane-to-lane alignment and clock rate compensation
- 8B/10B encoding to convert the binary data to 10-bit encoded data for each lane
- Supports loopback control of the SERDES PHY transmit to receive

Receive Path

- Lane synchronization on received side to determine code group boundaries
- De-skew of all received code groups to an alignment pattern with a maximum allowed skew over 5 cycles
- 10B/8B decoding per lane
- Link status reporting for faulty conditions
- Clock rate compensation in which idle characters are inserted or deleted to compensate for the frequency variations between the recovered clock and the local clock – maximum allowed variation between clocks is 200 ppm
- Optional conversion the single data rate (32-bit) at 312.5 MHz to double data width (64-bit) at 156.25 MHz
- Diagnostic logic for BER testing in compliance to the IEEE 802.3ae Annex 48A specification
- Supports XGMII internal loop back for debugging receive to transmit digital path
- MDIO Manageable Device (MMD)
- Error status and statistics for debug



The dwc_ether_xgxs_pcs datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_ether_xgxs_pcs.pdf

dwc_mobile_storage

Mobile Storage Host Controller

Core Features

- SD 2.00, SDIO 2.0, MMC 4.2, and CE-ATA 1.1
- Configured either as an MMC-only controller or SD_MMC controller
- 1-30 MMC cards in MMC-only mode, or 1-16 cards in SD_MMC mode
- SD_MMC mode supports CE-ATA
- Command Completion Signal and interrupts to host for CE-ATA
- Command Completion Signal disables CRC generation and checking in CE-ATA mode
- SD_MMC mode supports 1-bit, 4-bit, and 8-bit cards
- Programmable baud rates; supports up to four clock dividers for simultaneous operation of cards with different clock-speed requirements
- Card detection and write protection
- Host pullup control
- SDIO interrupts in 1-bit and 4-bit modes
- 1- to 65,535-byte blocks
- Suspend and resume operations
- Low-power system option with individual clock and power ON/ OFF features to each card
- Lane reversal and polarity inversion

Bus Interface Features

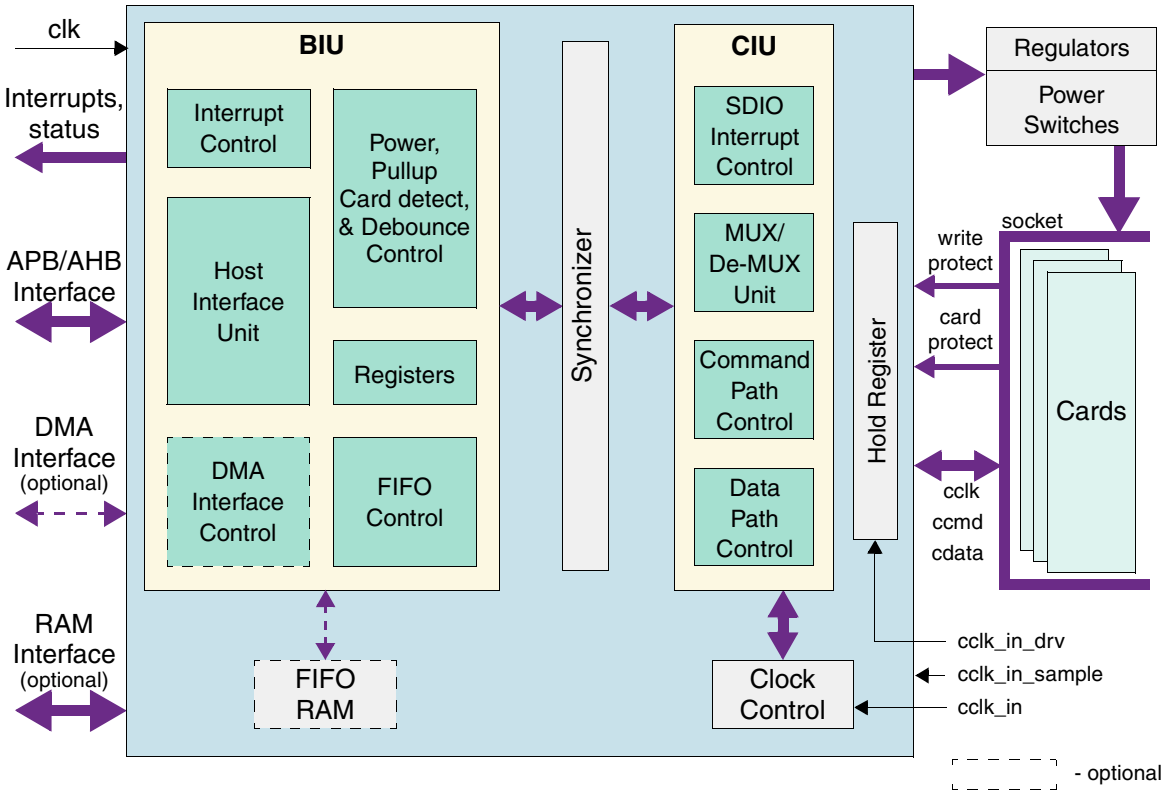
- Supports either AMBA 2.0 AHB or APB slave interfaces
- Supports 16-, 32-, or 64-bit data widths
- Supports descriptor-based DMA interface
- Separate clocks for bus interface and card interface for easy integration
- Supports 8- to 4096-deep configurable FIFO
- Single FIFO optimized for area and power savings without compromising performance
- Default register-based FIFO RAM, which can be replaced by FAB-specific dual-port SRAM
- Supports FIFO over-run and under-run prevention by stopping card clock
- In AHB mode, supports pin-based little-endian and big-endian modes

Verification Environment Features

- VMT-based AMBA bus-functional models and monitors
- VMT-based MMC, SDMem, SDIO, and SDCombo, CE-ATA BFMs can be used in VERA/Verilog Environment
- Exhaustive constrained random and directed testing
- Verified with AMBA Compliance Test
- 100% Line and FSM coverage
- 99.9% ATPG coverage
- SD MMC_CE-ATA independent SD/ MMC protocol-specific bus-drive APIs

Example Linux Demonstration Features

- SD-, MMC-, CE-ATA-specific host-driver APIs



The DesignWare DWC_mobile_storage datasheet is available at:

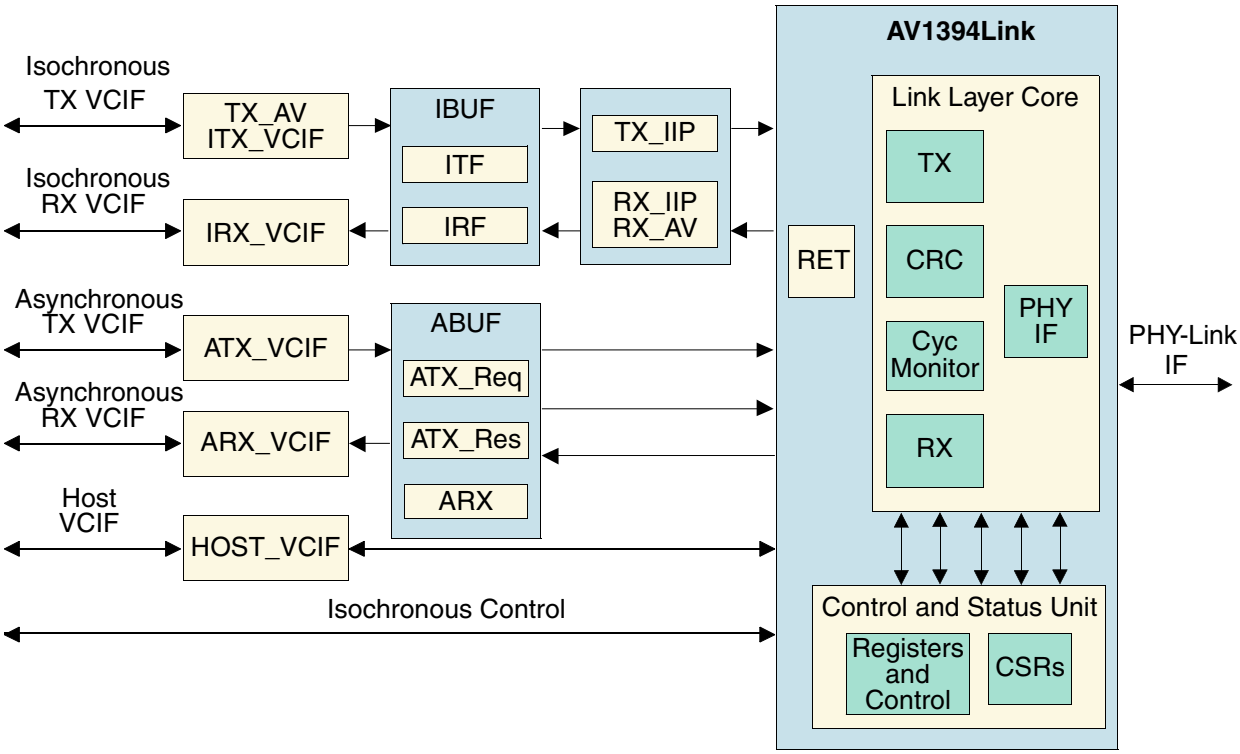
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_mobile_storage.pdf

dwc_1394_av_link

Synthesizable IEEE 1394 AVLink DTCP

The Synopsys DesignWare IEEE 1394 AVLink DTCP intellectual property (IP) is a set of highly configurable blocks that implements complete 1394 interface functions tailored to support audio/visual (AV)-oriented IEC 61883 applications. Configured through our RapidScript utility, this device can also be optimized to act as a generic 1394 device controller. Therefore, AVLink can be effectively used in a wide range of applications, such as digital still cameras, video conferencing cameras, printers, scanners, digital audio devices, electronic musical instruments, digital VCRs/VTRs, and storage devices. Other features include the following:

- Silicon-proven IEEE 1394 Link Layer Controller for both audio/visual (A/V) and non-A/V applications
- Support for common isochronous packet (CIP) headers, time-stamping, and padded zeros for A/V data transactions
- IEEE 1394-1995 and 1394a-2000 specification compliance
- IEC 61883 requirement for A/V data streaming compliance
- Supports 100/200/400- Mbps data rates
- Full link layer implementation
- Asynchronous, isochronous, and PHY packet transmit and receive operations
- Cycle master and node controller capability
- Automatic isochronous resource manager detection
- Automatic acknowledge packet generation for received asynchronous packets
- Automatic 32-bit CRC generation and error detection interface
- Flexible, 32-bit Virtual Component Interface (VCI) for host
- Asynchronous and isochronous FIFO interface with burst and non-burst access modes
- Multi-speed, concatenated isochronous packet support
- Configurable number of isochronous transmit/receive channels
- Status reporting by extensive maskable interrupt register set
- Supports inbound and outbound single phase retry protocol
- RapidScript custom IP configuration
- Verilog source code
- Optional 1394 verification environment



The dwcore_1394_avlink datasheet is available at:

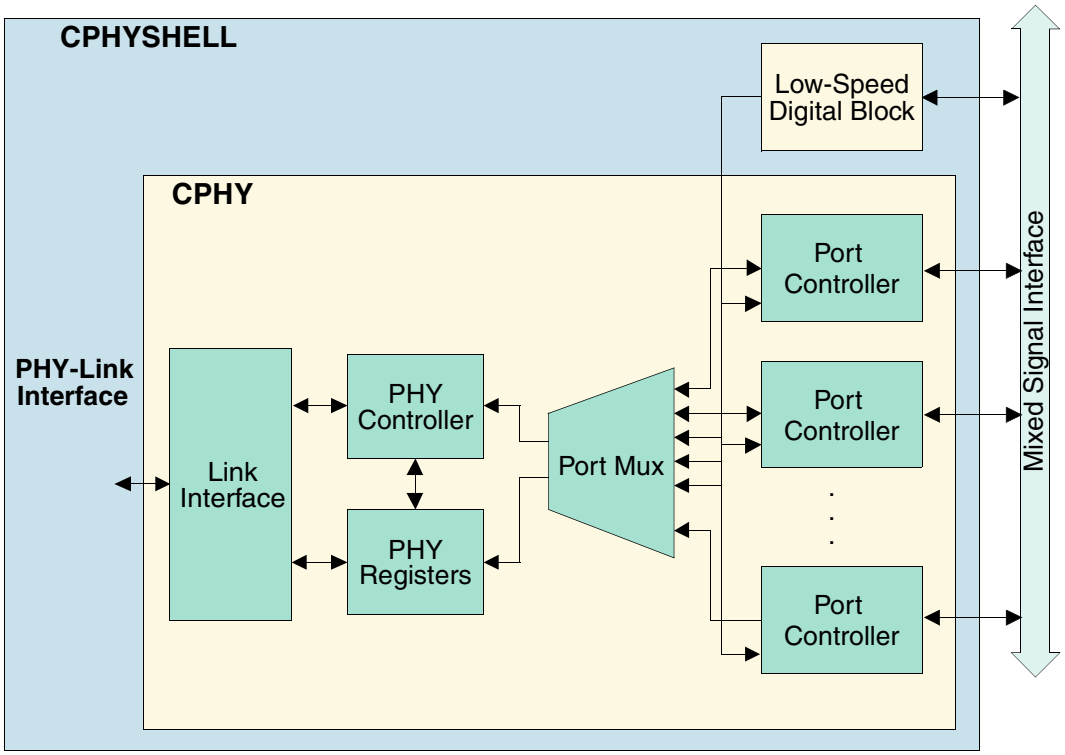
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_1394_av_link.pdf

dwc_1394_cphy-native

Synthesizable IEEE 1394 Cable PHY

The Synopsys industry-proven DesignWare 1394 Cable Physical Layer (CPHY) enables devices to interface with the 1394 serial bus. The 1394 CPHY is a synthesizable RTL design that provides all the necessary features to implement the complete IEEE 1394a specification for the digital portion of the cable PHY. CPHY can be combined with an analog PHY and used in a stand-alone ASIC, or it can be integrated into an ASIC with a Link Layer controller. CPHY is well suited for multimedia and mass storage applications requiring high bandwidth, and is suitable for a wide range of applications, from basic low-cost devices (1 port) to sophisticated, high-performance ASICs (up to 16 ports). Other features include the following:

- Complete IEEE 1394a support
- Supports 100/200/400-Mbps bus speeds
- Configurable number of ports (1 to 16)
- Simple, silicon-proven interface to mixed signal analog circuitry
- Supports suspend/resume protocol
- Supports Link-On LPS protocol
- RapidScript configuration utility for design customization
- Synthesis scripts
- Verilog source code
- Approximately 14K gates (3 port)
- Proven in ASIC applications



The dwcore_1394_cphy datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_1394_cphy-native.pdf

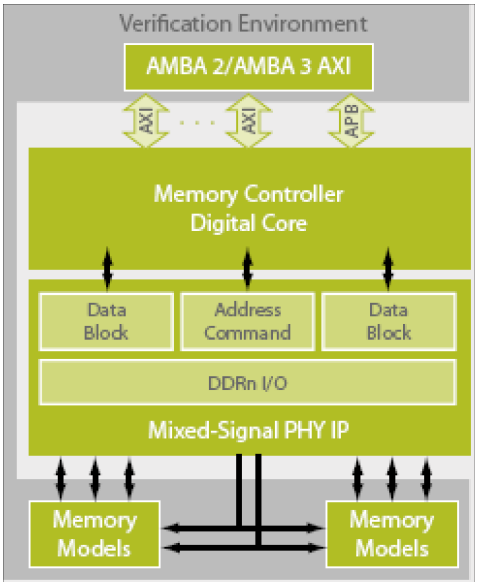
DDR2/3-Lite SDRAM Complete Solution

DDR2/3-Lite SDRAM Complete Solution

The DesignWare DDR2/3-Lite IP is a complete, silicon-proven, system-level IP interface solution for ASICs, ASSPs, System-on-Chip (SoC) and System-in-Package applications requiring highperformance DDR2/3 SDRAM interfaces operating at up to 1066 Mbps. The DDR2/3 Lite IP, part of the comprehensive DesignWare DDRn IP product line, is ideal for systems that do not require the higher performance or lower power consumption of DDR3. It is targeted at designs that are initially going to market using DDR2 IP with the ability to transition to DDR3 IP, should the equivalent DDR3 products become less expensive.

This transition from DDR2 to DDR3 can be implemented if the DRAMs used by the system are 512Mb devices or larger (1 Gb is the recommended minimum for the ultimate long term security of supply) because DDR3 devices are only offered in this range. In situations where the DDR3-based design requires performance levels of over 1066 Mbps, the DesignWare DDR3/2 IP product should be considered. Optimized for low area and power, the DesignWare DDR2/3-Lite SDRAM IP complete solution includes configurable digital controller IP, an integrated hard macro PHY and verification IP (VIP). The high quality, silicon-proven DDR2/3-Lite IP enables designers to focus on product differentiation and not on the memory subsystem design issues that are present as data rates exceed 400 Mbps, thus significantly reducing design integration risk and accelerating overall development time.

As part of the “Lite” DDR3 mandate for this product, the DDR3 write leveling feature is not implemented and thus this interface solution is not recommended for those applications that require an interface to DDR3 DIMMs.



Highlights

Solution

- Complete DDR2/3 SDRAM Memory Interface IP solution, including digital controller, PHY, and VIP
- Services data rates up to 1066 Mbps
- Area optimized PHY IP for lower performance range of DDR3
- Integrated solution eases timing closure with optimized interface between PHY and controller
- PHY IP is available in leading 65nm process technologies

Digital Controller

- DDR2/3-Lite PHY IP is compatible with DesignWare Protocol (PCTL) and Memory Controller (MCTL)
- Automatic scheduling of activate and precharge commands (PCTL, MCTL)
- Automatic scheduling of refreshes (PCTL, MCTL)
- Advanced command re-ordering and scheduling to maximize bus utilization (MCTL)
- Configurable multi-port arbiter supporting multiple independent user ports (MCTL)
- Programmable ECC generation, checking, and correction (MCTL)
- Supports AMBA AXI and Native Interface (NIF) (PCTL, MCTL)

PHY IP

- Configurable PHY IP easily goes around die corner
  - PHY IP compiler available
  - Lane-based PHY IP architecture for maximum flexibility
- Precision master/slave delay locked loops (DLLs) provide 90o phases of the clock/strobes
  - Automatic calibration
  - Immune to voltage and temperature drift
  - Ultra-low jitter
- Per bit timing adjustment on data and strobe signals to improve timing margin
- Data training for DQS gating
- Real time DQS drift detection and compensation
- PVT compensated I/Os using DDR3 ZQ pad with external precision resistor
  - Calibrates output drive impedance and ODT

The product datasheet can be downloaded from the following site:

http://www.synopsys.com/designware

DDR2/DDR SDRAM PHY and Controller

DDR2/DDR SDRAM Complete Solution

The DesignWare IP for DDR2/DDR interfaces is a complete, silicon-proven, system-level IP interface solution for ASICs, ASSPs, System-on-Chip (SoC) and System-in-Package applications requiring high-performance DDR2/DDR SDRAM interfaces operating at up to 1066 Mpbs. This silicon proven DDR2/DDR SDRAM complete solution includes scalable digital controller IP, an integrated hard macro PHY and verification IP. The pre-qualified and interoperable interface unburdens developers from memory subsystem design issues that come into play when memory data rates move beyond 400 Mbps, enabling them to focus their energy on value-added development, while significantly reducing design risk and development time.

Highlights

Solution

- Complete, integration DDR2/DDR SDRAM Memory Interface solution including digital controller, PHY and verification IP
- High performance, operating at up to 1066 Mbps
- Integrated solution eases timing closure with optimized interface between PHY and controller
- Silicon-proven PHYs are available in leading 65nm, 90nm and 130nm process technologies

Digital Controller

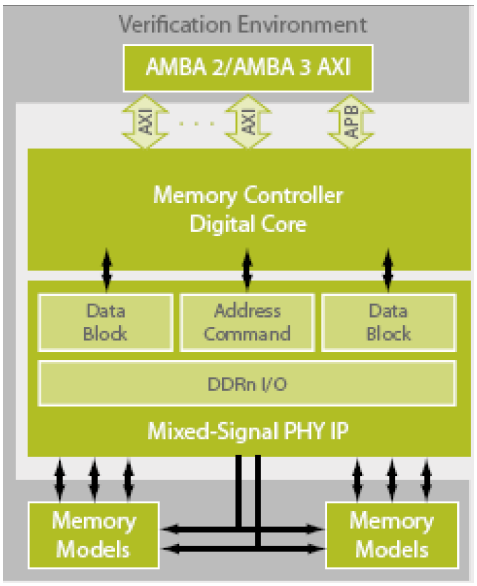
- Advanced command re-ordering and scheduling to maximize bus utilization
- Automatic scheduling of activate and precharge commands
- Automatic scheduling of refreshes
- Configurable multi-port arbiter supporting multiple independent user ports
- Configurable quality of service capability per user port
- Programmable ECC generation, checking, and correction
- Supports ARM AMBA AXI & AHB protocols
- Real time DQS drift detection and compensation

PHY IP

- Configurable PHY easily goes around die corner
  - PHY compiler available
  - Lane based PHY architecture for maximum flexibility
- Precision master/slave DLLs provide 90^{o} phases of the clock/strobes
  - Automatic calibration
  - Immune to voltage and temperature drift
  - Ultra-low jitter
- Per bit timing adjustment on data and strobe signals to improve timing margin
- Data training for DQS gating

Verification IP

- Verifies complete memory system with verification IP of physical memories (memory models) and on-chip interfaces (AXI and OCP)
- Provides directed and constrained random traffic generation
- Supports major simulators and testbench languages including Verilog, SystemVerilog, OpenVera and VHDL



The product datasheet can be downloaded from the following site:

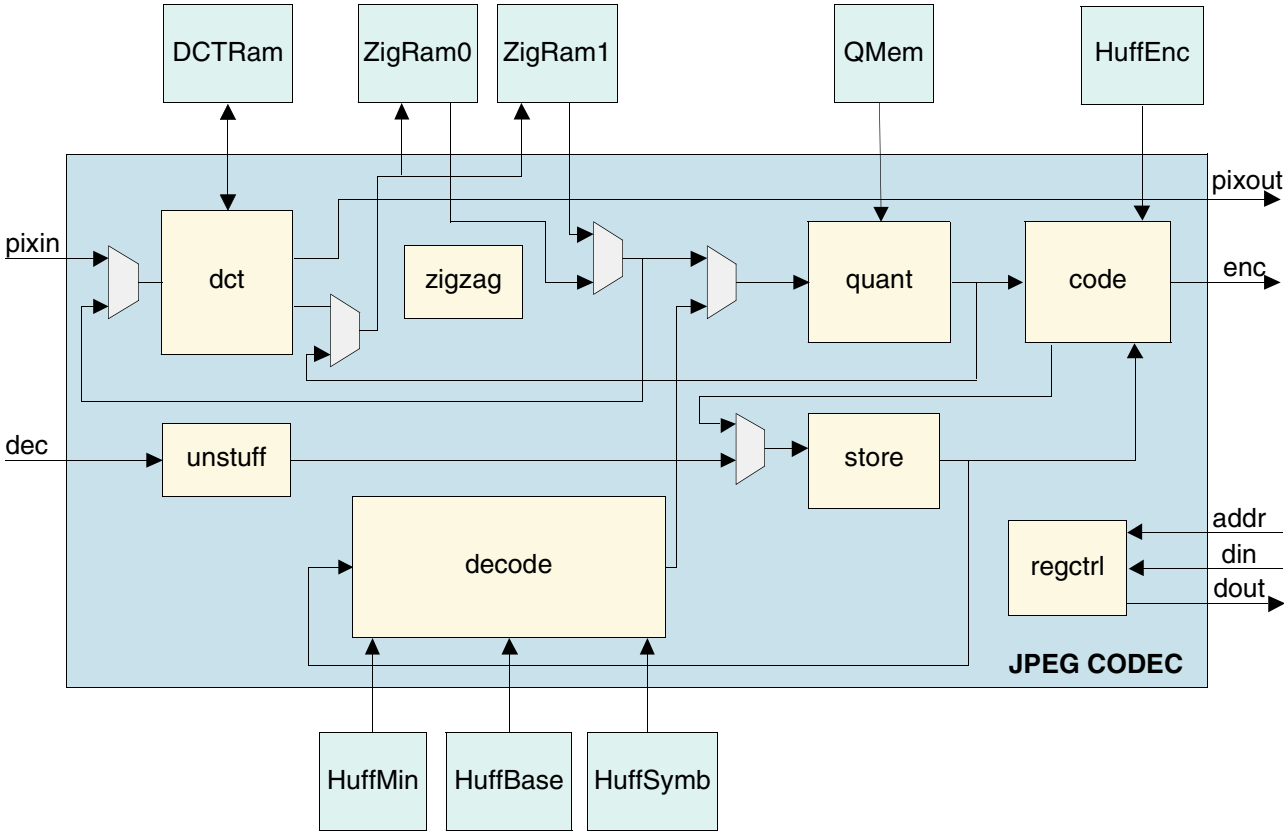
http://www.synopsys.com/designware

dwc_jpeg

Synthesizable JPEG CODEC

The Synopsys DesignWare JPEG CODEC is part of an SoC-based multimedia solution that enables fast and simple image compression and decompression. The simplicity of the design allows for easy SoC integration, high-speed operation, and suitability for multimedia and color printing applications. Individual Encoder and Decoder products are available from Synopsys. Other JPEG CODEC features include the following:

- 100% baseline ISO/IEC 10918-1 JPEG-compliant
- Verified in hardware
- 8-bit channel pixel depths
- Up to four programmable quantization tables
- Single-clock Huffman coding and decoding
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable Minimum Coded Unit (MCU)
- Encoding/decoding support (non-simultaneous)
- Single-clock per pixel encoding and decoding according to the JPEG baseline algorithm
- Hardware support for restart marker insertion
- Support for single, grayscale components
- Support for up to four channels of component color
- Internal register interface
- Fully synchronous design
- Available as fully functional and synthesizable VHDL or Verilog
- Includes testbench
- Simple external interface
- Four-channel interface
- Low gate count-total gate count is 35K gates
- Stallable design



The dwcore_jpeg_codec datasheet is available at:

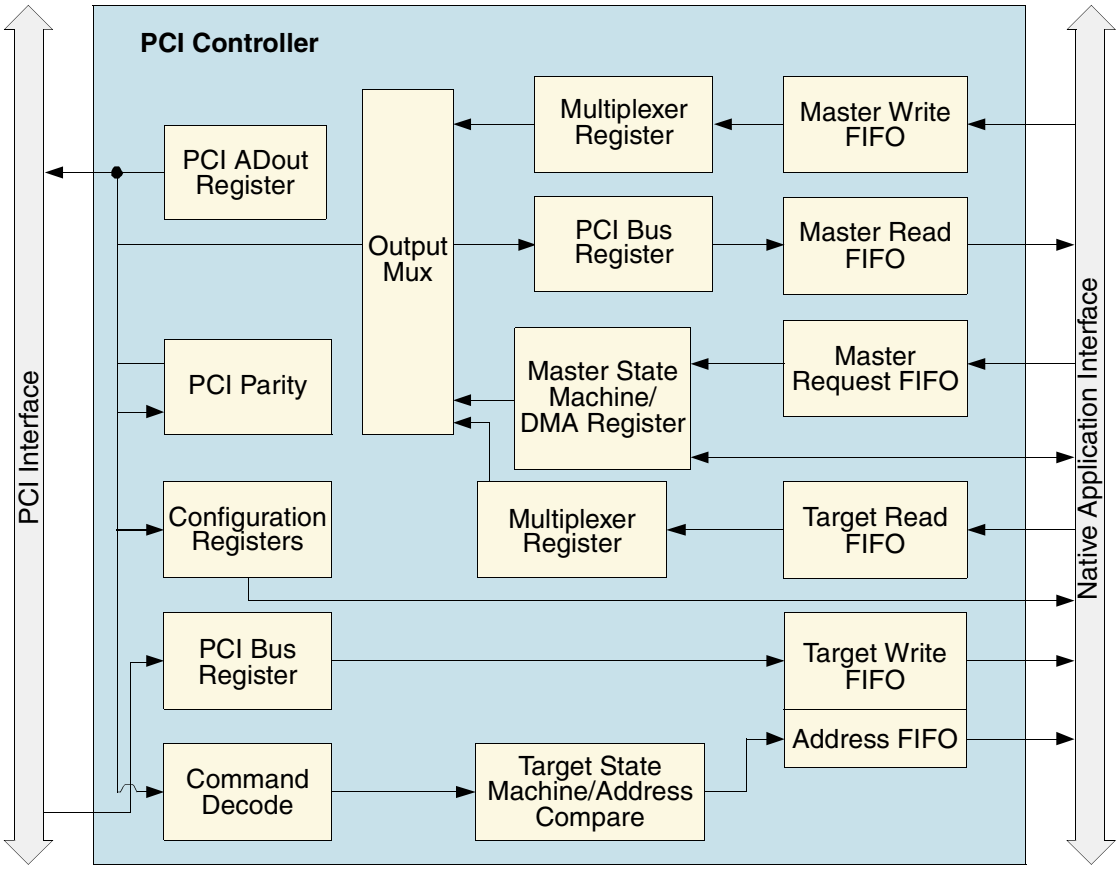
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_jpeg.pdf

dwc_pci

Universal PCI Controller

The DesignWare IP core for PCI is available as synthesizable RTL source code and provides an interface between the application and the PCI bus. Some of the key features include the following:

- PCI specification 2.3 compliant
- 15 application-optimized PCI IP, available in Verilog
- Silicon-proven 33-MHz and 66-MHz performance
- 32-bit or 64-bit PCI bus path
- 32-bit or 64-bit application data path
- Zero Latency, Fast Back-to-Back transfers
- Zero Wait-State Burst Mode transfers
- Support for Memory Read Line/ Multiple and Memory Write and Invalidate commands
- Dual Address cycles
- Loadable configuration space
- Universal configuration optimized for use in both Host Bridge and Add-in Card designs
- Delayed Read support
- PCI power management support
- PCI multifunction support



The dwcore_pci datasheet is available at:

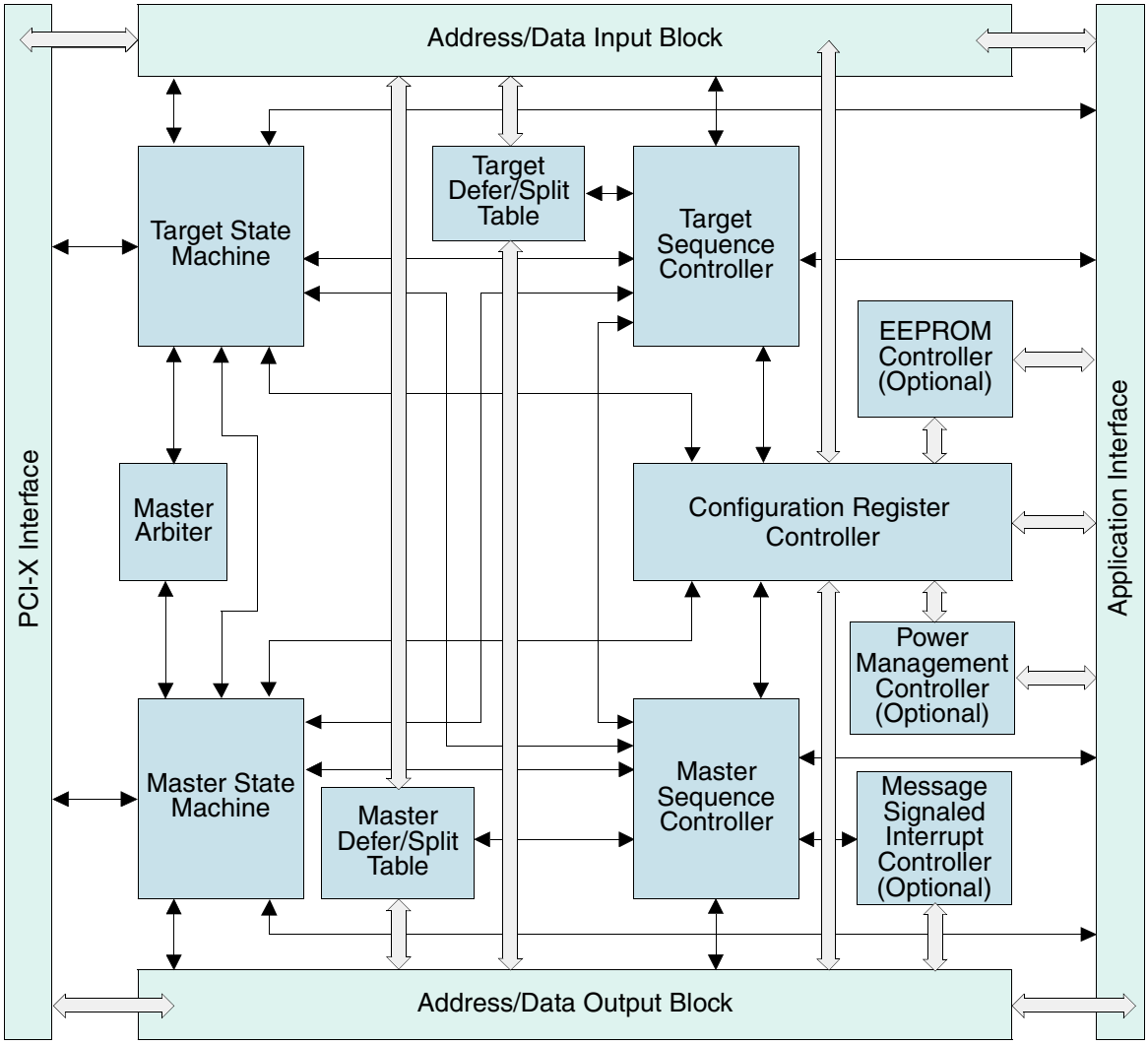
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_pci.pdf

dwc_pci-x

Synthesizable PCI-X Controller and Test Environment

The DesignWare IP core for PCI-X is available as synthesizable RTL source, which enables designers to implement a complete PCI-X interface. PCI-X is highly suitable in a wide range of applications, such as SCSI, Fibre Channel, Gigabit Ethernet, and graphics. Other features include the following:

- PCI-X 1.0a compliant
- Host Bridge functionality
- PCI 2.3 compliant
- 32-bit or 64-bit PCI-X bus path
- 64-bit application data path
- Supports 0-133 MHz PCI-X bus
- Supports up to 32 outstanding delayed/split transactions
- Dual Address Cycles (DAC)
- Message Signaled Interrupts (MSI)
- External EEPROM support
- Comprehensive Test Environment — Device Under Test linkable to the test environment
- RapidScript parameterized configuration for fast customization
- Synthesizable Verilog source code



The dwcore_pcix datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_pci-x.pdf

PCIe-AHB Bridge

PCI Express to AMBA 2.0 AHB Bridge

The DesignWare PCI Express to AMBA 2.0 AHB Bridge (PCIe-AHB Bridge) enables designers who use the AMBA 2.0 AHB on-chip bus to easily add PCI Express external connectivity to their AMBA 2.0 AHB-bases System-on-Chip (SoC) devices. Other features include the following:

- AHB Master and Slave interfaces for inbound and outbound PCI Express requests
- Supports full PCI Express configuration, I/O requests, traffic class (EP, TD, etc.) through PCIe-AHB Bridge
- AHB Slave interface for PCI Express core CDM register access through the PCI Express core's DBI interface
- Programmable buffer sizes for AHB Master and Slave requests and response queuing
- Independent programmable clock rates for the PCI Express core and AHB subsystem
- Programmable maximum number of inbound and outbound read requests for AHB
- All burst-sizes supported for both AHB Master and Slave interfaces
- Programmable burst lengths to support 4K read/write burst over AHB Master and Slave interfaces
- Independent maximum read request and transfer sizes between AHB and PCI Express (transfers can be split into multiple transfers)
- Response AHB Slave request gathering from split PCI Express completions
- Response AHB Master request gathering from multiple AHB responses
- Out-of-order transactions for transactions with unique Master IDs
- Interrupt and Message handling
- Response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AHB Slave response errors
- Response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AHB Master response error
- PCIe-AHB Bridge handles completion time outs

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

PCIe-AXI Bridge

PCI Express to AMBA 3 AXI Bridge

The DesignWare PCI Express to AMBA 3 AXI Bridge (PCIe-AXI Bridge) enables designers who use the AMBA 3 AXI on-chip bus to easily add PCI Express external connectivity to their AMBA 3 AXI-bases System-on-Chip (SoC) devices. Other features include the following:

- AXI Master and slave interfaces for inbound and outbound PCI Express requests
- Supports full PCI Express configuration, I/O requests, traffic class (EP, TD, etc.) through PCIe-AXI Bridge
- AXI Slave interface for PCI Express core CDM register access through the PCI Express core's DBI interface
- Independent configuration of bus width for PCI Express core data bus, AXI master bus and AXI slave bus
- Programmable buffer sizes for AXI master and slave requests and response queuing
- Independent programmable clock rates for the PCI Express core, the AXI master bus, the AXI slave bus and the AXI slave DBI bus
- Programmable AXI master and slave address widths, data bus widths, and ID bus widths
- Programmable maximum number of inbound and outbound read requests for AXI
- All burst-sizes supported for both AXI master and slave interfaces
- Programmable burst lengths to support 4K read/write burst over AXI master and slave interfaces
- Supports unaligned AXI transfers using WSTRB and RTSRB for both AXI master and slave interfaces
- Supports independent maximum read request and transfer sizes between AXI and PCI Express (transfers can be split into multiple transfers)
- Supports response AXI slave request gathering from split PCI Express completions
- Supports response AXI master request gathering from multiple AXI responses
- Supports out-of-order transactions for transactions with unique IDs
- Supports Interrupt and Message handling
- Supports response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AXI slave response errors (SLVERR and DECERR)
- Supports response error mapping between PCI Express errors (UR, CA, CRS, poisoned, and ECRC error) and AXI master response error (DECERR_W and DECERR_R)
- Support for byte parity check for the address and data buses though the PCIe-AXI Bridge
- PCIe-AXI Bridge handles completion time outs

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

dwc_pci_express_ep

PCI Express Endpoint Synthesizable Core

The DesignWare Endpoint Core for PCI Express implements the port logic required to build a PCI Express 2.0 Endpoint device. The silicon-proven Endpoint core is configurable and scalable to meet multiple endpoint application requirements ranging from server and desktop systems to mobile devices.

Other features include the following:

- Complies to PCI Express Base Specification, Revision 2.0
- Modular design, including a base core (CXPL) plus additional support modules for Endpoint-specific functionality
- Type 0 configuration space
- 62.5Mhz/125MHz/250MHz/500Mhz
- Up to 16 2.5/5.0-Gbps Lanes (x1, x2, x4, x8, or x16)
- 32, 64, or 128-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Very high accessible bandwidth
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple functions
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- Configurable for infinite credits for all types of traffic
- ECRC generation and checking
- PCI Express beacon and wake-up mechanism
- PCI power management
- PCI Express Active State Power Management (ASPM)
- PCI Express Advanced Error Reporting
- MSI and MSI-X
- All in-band Messages for PCI Express Endpoint
- Configurable Endpoint filtering rules for Posted, Non-Posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, and configuration filtering
- Programmable completion timeout

- Supports up to three independent client interfaces for transmitting TLPs
- Access to configuration space registers and external application registers through local bus controller
- Automatic generation of Completions for devices that require only simple access to an application register block
- Selectable arbitration mechanism for transmit interfaces, or use an external arbiter
- Supports expansion ROM
- Implements parity checking on transmit buses, memory buses, and internal data buses (optional)

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

dwc_pci_express_rc

PCI Express Root Port Synthesizable Core

The DesignWare Root Port core for PCI Express 2.0 is a synthesizable RC solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices. Other features include the following:

- Complies to PCI Express Base Specification, Revision 2.0
- Modular design, including a base core (CXPL) plus additional support modules for Root Port-specific functionality
- Type 1 configuration space
- 62.5MHz/125MHz/250MHz/500MHz
- Up to 16 2.5/5.0-Gbps Lanes (x1, x4, x8, or x16)
- 32, 64, or 128-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Very high accessible bandwidth
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- Application-initiated Lane reversal for situations where the EP Core does not detect Lane 0 (for example, an x4 EP Core connected to an x8 device that has its Lanes reversed
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple functions
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- Configurable for infinite credits for all types of traffic
- Supports ECRC generation and checking
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI power management
- Supports PCI Express Active State Power Management (ASPM)
- Supports PCI Express Advanced Error Reporting
- Supports all in-band Messages for PCI Express Root Port
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic
- Supports two application transmit clients by default, additional third client optional
- Access to configuration space registers from the application through the DBI

- Automatic generation of Completions for Requests that require Unsupported Request (UR) or Completer Abort (CA) responses
- Supports external priority arbiter (in addition to the internally-implemented transmit arbitration)
- Supports expansion ROM
- Implements parity checking on transmit buses, memory buses, and internal data buses (optional)

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

dwc_pci_express_sw

PCI Express Switch/Bridge Synthesizable Core

The DesignWare Switch/Bridge core for PCI Express 2.0 is a synthesizable SW solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices. Other features include the following:

- Complies to PCI Express Base Specification, Revision 2.0
- Modular design including a base core (CXPL) plus additional support modules for Switch-specific functionality
- Type 1 configuration space
- 62.5MHz/125MHz/250MHz/500MHz
- Up to 16 2.5/5.0-Gbps Lanes (x1, x4, x8, or x16)
- 32, 64, or 128-bit datapath width
- Configurable as upstream Switch Port, downstream Switch Port, PCI(-X) to PCI Express Bridge, or PCI Express to PCI(-X)
- Full PCI Bridge-to-Bridge support
- Support for 8-bit and 16-bit PHYs through the PIPE
- Supports prefetchable memory space
- Transaction filtering and routing look up
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Configurable VC/TC mapping
- Full PCI Express Message passing and processing
- Ultra low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Very high accessible bandwidth
- Lane reversal (transmit and receive)
- Polarity inversion (transmit and receive)
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- Configurable for infinite credits for all types of traffic
- Supports ECRC checking and error reporting (optional)
- Supports PCI Express beacon and wake-up mechanism
- Supports PCI power management
- Supports PCI Express Active State Power Management (ASPM)
- Supports PCI Express Advanced Error Reporting
- Full PCI Express Message passing and processing
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic

- Configurable BAR filtering, I/O filtering, configuration filtering
- Supports two application transmit clients by default, additional third client optional
- Access to configuration space registers and external application registers through local bus controller
- Supports external priority arbiter (round robin used for internal arbitration)
- Supports expansion ROM
- Implements parity checking on transmit buses, memory buses, and internal data buses (optional)

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

dwc_pci_express_dm

PCI Express RC/EP Dual Mode Synthesizable Core

The DesignWare Dual Mode (Root Port/Endpoint) Core for PCI Express 2.0 is a synthesizable solution that can be configured to address multiple applications, ranging from server and desktop systems to mobile devices. Other features include the following:

- Complies to PCI Express Base Specification, Revision 2.0
- Modular design, including a base core (CXPL) plus additional support modules for Endpoint-specific functionality
- Operating mode (EP or RC) determined by state of input pin at power-on reset
- Type 0 configuration space in EP mode; type 1 configuration space in RC mode
- 62.5MHz/125MHz/250MHz/500MHz
- Up to 16 2.5-Gbps Lanes (x1, x2, x4, x8, or x16)
- 32, 64, or 128-bit datapath width
- Support for 8/16/32-bit PHYs through the PIPE
- Ultra-low transmit and receive latency
- Configurable retry buffer size
- Configurable number of outstanding Requests
- Configurable Max_Payload_Size size (128 bytes to 4 KB)
- 4-KB maximum Request size
- Very high accessible bandwidth
- Automatic Lane reversal as specified in the PCI Express Base Specification (transmit and receive)
- In RC mode: application-initiated Lane reversal for situations where the EP Core does not detect Lane 0 (for example, an x4 EP Core connected to an x8 device that has its Lanes reversed)
- Polarity inversion on receive
- Multiple Virtual Channels (VCs)
- Multiple Traffic Classes (TCs)
- Multiple functions
- Supports bypass, cut-through, and store-and-forward queues for received TLPs
- Configurable for infinite credits for all types of traffic
- ECRC generation and checking
- PCI Express beacon and wake-up mechanism
- PCI power management
- PCI Express Active State Power Management (ASPM)
- PCI Express Advanced Error Reporting
- MSI and MSI-X
- All in-band Messages for the current mode (EP or RC)
- Configurable filtering rules for Posted, Non-Posted, and Completion traffic

- Configurable BAR filtering, I/O filtering, and configuration filtering
- Programmable completion timeout
- Supports up to three independent client interfaces for transmitting TLPs
- Access to configuration space registers and external application registers through local bus controller
- Automatic generation of Completions for devices that require only simple access to an application register block (EP mode)
- Automatic generation of Completions for Requests that require Unsupported Request (UR) or Completer Abort (CA) responses (RC mode)
- Selectable arbitration mechanism for transmit interfaces, or use an external arbiter
- Supports expansion ROM
- Implements parity checking on transmit buses, memory buses, and internal data buses (optional)

More information is available at:

http://www.synopsys.com/products/designware/pciexpress.html

dwcore_pcie_phy

PCI Express PHY IP

The DesignWare PCI Express PHY IP integrates high-speed mixed-signal custom CMOS circuitry for easy integration into system-on-chip designs. The high-margin, robust PCI Express PHY architecture tolerates manufacturing variations such as process, voltage, and temperature.

While extremely low in power (up to 50% less than conventional PHYs) and area, the DesignWare PCI Express PHY substantially exceeds the electrical specifications defined in the PCI Express base specification in key performance areas such as jitter and receive sensitivity.

The unique, advanced, built-in diagnostics and ATE test vectors available in the DesignWare PCI Express PHY enables designers to implement complete at-speed production testing without the need for expensive test equipment. Furthermore, the PCI Express PHY provides on-chip visibility into the actual link performance and quickly identifies signal integrity issues. This method is superior to the traditional “loopback” mechanism.

PHY Features

- Fully complies with PCI Express 1.1 (2.5 Gbps) and 2.0 (5.0 Gbps) specifications
- Complies with 1.87 PIPE specification
- Supports popular 65-,90-,and 130-nm processes in multiple foundries
- 8- and 16-bit PIPE PHY interfaces
- Supports x1, x4, and x8 lanes
- Supports all power-down modes and spread spectrum clocking
- Supports beaconing, receiver detection, and electrical idle
- Provides excellent performance margin and receive sensitivity
- Consumes very low power (up to half the power compared to conventional PCIe® PHYs)
- Occupies very small die size (up to half the size of conventional PCIe PHYs)
- Provides robust PHY architecture and tolerates wide PVT variations
- Supports flip-chip and low-cost wirebond packages
- Implements low-jitter PLL technology with excellent supply isolation
- Provides low-offset, high-sensitivity receiver with high-resolution CDR
- Supports ± 10% supply variation
- Uses 100-MHz, 125-MHz, and 156.25-MHz reference clocks

Verification Features

- Supports verification at PIPE, 10b, and serial interface
- Supports automatic handling of transaction, data link and physical layer tasks
- Provides full Requester and Completer functions
- Supports up to eight virtual channels
- Supports full LTSSM (Link Training)
- Supports power management
- Supports automatic generation of flow control packets
- Supports single word read and write transfers to memory, I/O, and configuration space
- Supports block read and write transfers to memory space
- Supports message transfers
- Supports orders packets based on PCI Express ordering rules
- Supports transaction reordering and out-of-order completions
- Supports modification and review of internal address spaces with zero cycle commands
- Supports error injection at each layer
- Provides functional coverage of PCI Express packet types

More information is available at:

http://www.synopsys.com/products/designware/docs/ds/c/dwc_pcie_phy.html

dwc_sata_ahci
Serial ATA AHCI

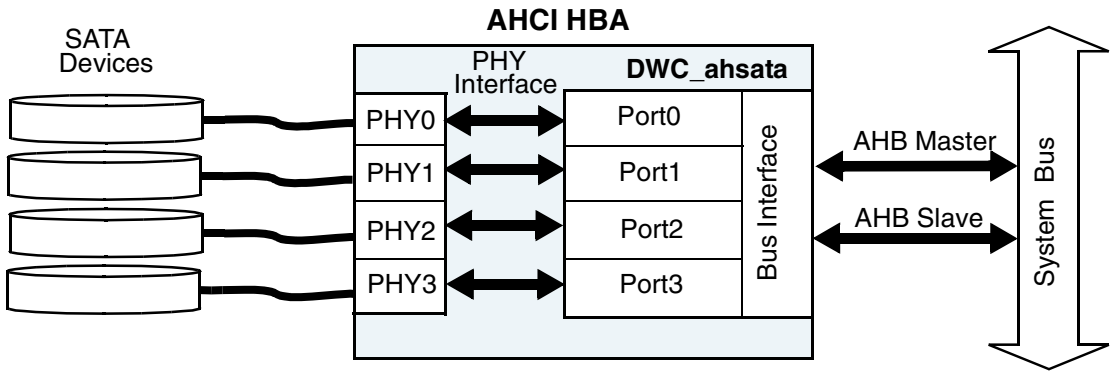
The DesignWare SATA AHCI intellectual property (IP) is designed for use in system-on-chip (SoC) solutions. The IP uses the popular AHB standard for a host interface and a configurable PHY/link interface to support a number of industry PHYs. Synopsys provides a large set of parameters to enable the IP's integration in systems with different requirements. By leveraging these parameters, the DWC SATA AHCI can optimize gate count and reduce time to market.

Features

- Supports SATA 1.5 Gbps Generation 1 and 3 Gbps Generation 2 speeds
- Compliant with Serial ATA Specification 2.6, and AHCI Revision 1.1 specifications
- Highly configurable PHY interface
- Provides additional user defined PHY status and control ports
- Optional Rx Data Buffer for recovered clock systems
- Optional data alignment circuitry when Rx Data Buffer is also included
- Optional OOB signalling detection and generation
- Gen2 speed negotiation when Tx OOB signalling is selected
- Digitally supports device hot-plugging when Tx OOB signalling is selected
- Optional 8b/10b encoding/decoding

Features

- Supports power management features
- Supports BIST loopback modes
- Supports up to 8 SATA devices (configurable from 1 to 8 ports)
- Configurable AMBA AHB interface (one master and one slave)
- Internal DMA engine per port
- Supports hardware-assisted Native Command Queuing for up to 32 entries
- Supports 64-bit addressing
- Supports Port Multiplier with command-based switching
- Optional mechanical presence switch, cold presence detect, and activity LED support
- Supports disabling Rx and Tx Data clocks during power down modes



The DesignWare dwc_sata_ahci datasheet is available at:

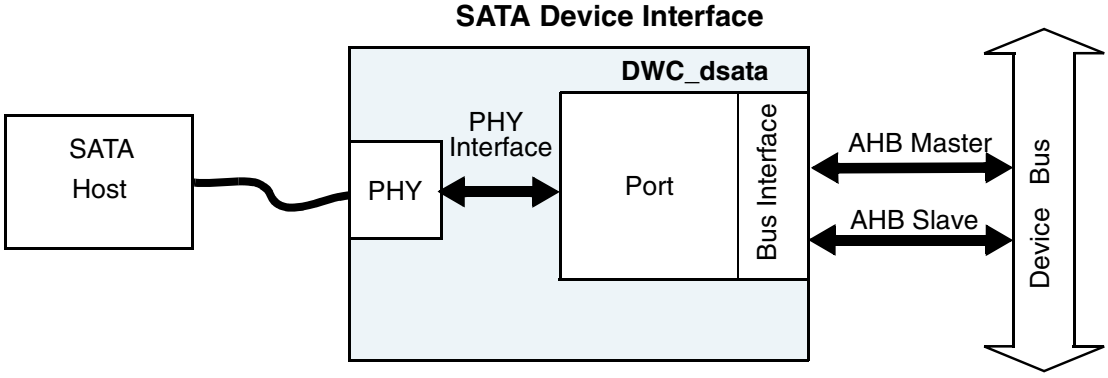
http://www.synopsys.com/products/designware/docs/ds/c/dwc_sata_ahci.pdf

DWC_dsata
Serial ATA Device

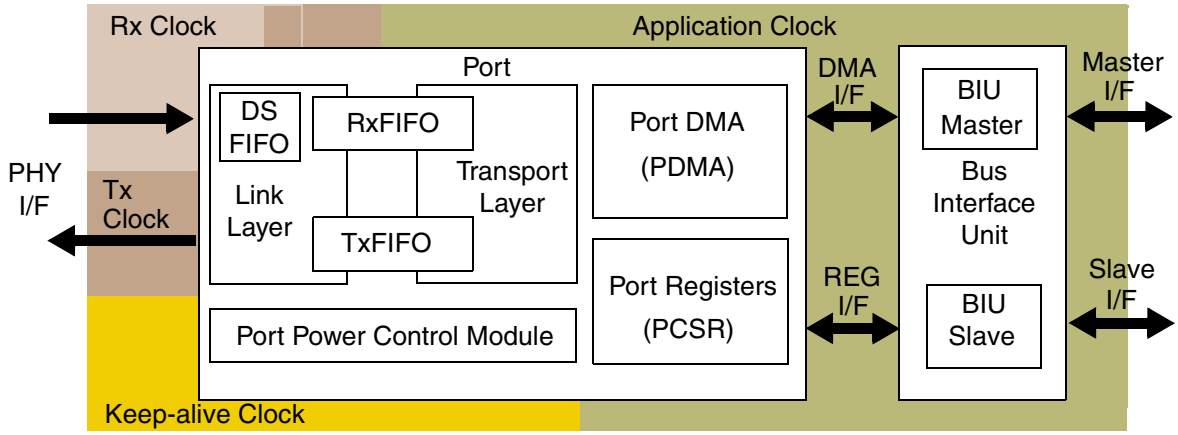
The DesignWare® IP for Serial ATA (SATA) Device Core is compliant to the SATA 2.6 specification for 1.5 and 3 Gb/sec and the draft SATA 3.0 specification for 6Gb/sec operation ensuring scalability and reuse in your current and future SoC. The digital device core offers a well defined, flexible programming model that minimizes software overhead during data transfers ensuring maximum operational performance. Sample device firmware for various applications is available on request. With its integrated DMA this high speed operation is achieved without additional system overhead. The core configuration offers one-click integration with the DesignWare IP SATA PHY removing the effort of integrating the digital and mixed signal portions of the SATA interface design. Reduced gate count and very low power consumption is achieved by utilizing the set of highly configurable options which enable the core to optimized based on the exact design requirements. The test environment for the digital device controller IP includes a number of the DesignWare Verification IP components offering SATA transactions generation, SATA protocol monitoring and AMBA subsystem transaction generation. Verilog-based tests are provided as examples to accelerate system integration.

- Compliant SATA Device for any application, HDD, ODD, SSD….
- Supports 1.5 Gb/sec, 3.0 Gb/sec and 6.0 Gb/sec speeds
- Compliant with SATA 2.6 specification (Draft 2.7 for 6Gb/sec)
- Internal DMA engine with flexible programming model
- Included Example Command Layer firmware
- Optional RX Buffer (elasticity buffer) for recovered clock systems
- Optional 8B/10B encoding/decoding
- Optional OOB detection/generation logic
- Data scrambling
- Speed negotiation when TX OOB signaling is enabled
- Full Power Management Features Supported
- Supports SATA defined BIST Modes
- Configurable AMBA System Interface
- Supports disabling of RX and TX clocks during power modes
- Highly configurable PHY interface
- Additional, user defined PHY status and control ports
- Validated against Synopsys and other PHYs

SATA Device Interface



DWC_dsata



The DesignWare DWC_dsata datasheet is available at:

http://www.synopsys.com/products/designware/docs/ds/c/dwc_sata_csds.pdf

dwc_sata_phy

Serial ATA PHY IP

The DesignWare SATA PHY IP integrates high-speed, mixed-signal, custom CMOS circuitry for easy integration into SoC designs. The high-margin, robust SATA PHY architecture tolerates manufacturing variations such as process, voltage, and temperature. The DesignWare SATA PHY integrates seamlessly with the DesignWare SATA Host core to help reduce design time and achieve first-pass silicon success. While extremely low in power consumption and area, the SATA PHY is compliant with the SATA 2.6 specification and substantially exceeds its electrical specifications in key performance areas such as jitter and receive sensitivity.

The unique, advanced, built-in diagnostics and ATE test vectors available in the DesignWare SATA PHY enables designers to implement complete at-speed production testing without the need for expensive test equipment. Furthermore, the DesignWare SATA PHY provides on-chip visibility into the actual link performance and quickly identifies signal integrity issues. This method is superior to the traditional “loopback” mechanism.

PHY Features

- Provides excellent performance margin and receive sensitivity
- Implements very low power design, up to half the power compared to conventional PHYs
- Provides ATE test vectors for complete at-speed production testing
- Includes on-board scope and diagnostics for fast system verification
- Supports popular 130-nm, 90-nm, and 65-nm processes
- Occupies small, cost-effective die size
- Supports hot-pluggable devices
- Implements low-jitter PLL technology with excellent supply isolation
- Provides low-offset, high-sensitivity receiver with high resolution
- Implements robust architecture that tolerates wide PVT variations

Test Features

- Provides built-in, per-channel BERTs
- Supports flexible, fixed and random pattern generation
- Supports error counting on patterns or disparity
- Supports digital phase or voltage margining (bathtub curves)
- Provides built-in, per-channel scopes for capture of eye diagram or coherent capture of periodic signals
- Supports loopbacks: serial analog (for wafer probe) and digital Tx to Rx
- Supports full analog ATE test on low-cost digital tester using only pass/fail JTAG vectors

The DesignWare dwc_sata_phy datasheet is available at:

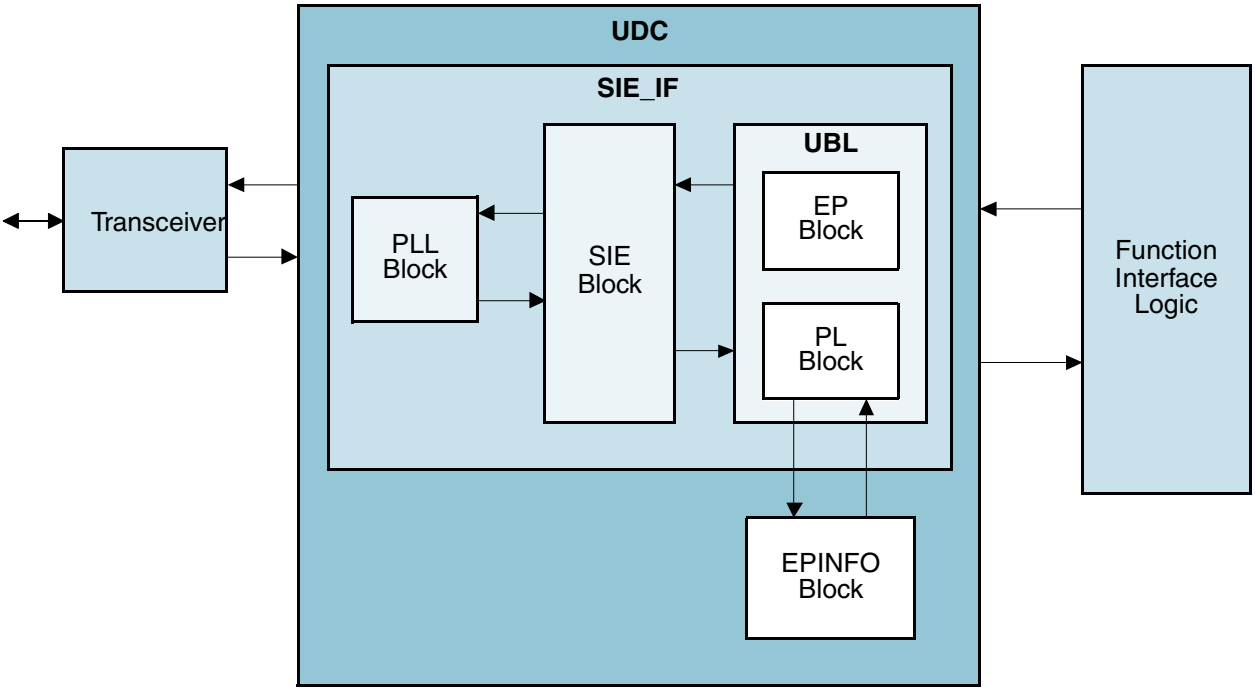
http://www.synopsys.com/products/designware/docs/ds/c/dwc_sata_phy.pdf

dwc_usb_1_1_device

Synthesizable USB 1.1 Device Controller

The Synopsys DesignWare USB Device Controller (UDC) is a set of synthesizable building blocks for implementing a complete USB device interface. Features include the following:

- 32-bit Virtual Component Interface (VCI)
- Maintains address pointer for endpoint 0 transactions
- Silicon proven
- USB 2.0 Full Speed compatible
- AMBA High-Performance Bus (AHB) interface enables rapid integration into ARM-based designs.
- Option to include internal DMA or interface to external DMA controller.
- Standard register set specification available
- Applications supported include: pointing devices, scanners, cameras, faxes, printers, speakers, monitor
- Verilog source code
- Supports low-speed and full-speed devices
- Programmable number of endpoints
- Easily configurable endpoint organization
- Supports up to 15 configurations, up to 15 interfaces per configuration, and up to 15 alternate settings per interface
- Supports all USB standard commands
- Easy-to-add Vendor/Class commands
- Suspend/resume logic provided
- Approximately 12K gates for 5 physical endpoints



The dwcore_usb1_device datasheet is available at:

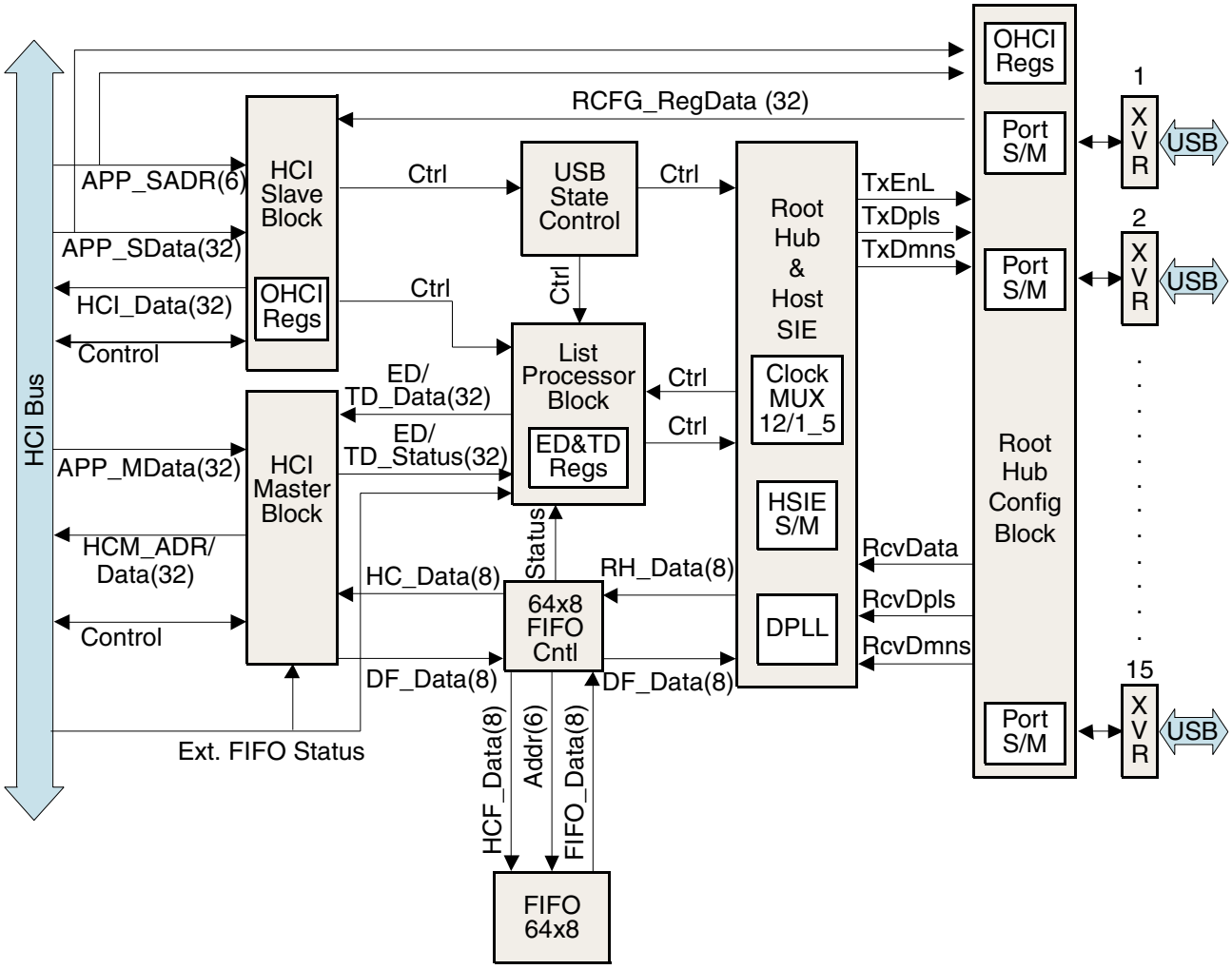
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb_1_1_device.pdf

dwc_usb_1_1_ohci_host

Synthesizable USB 1.1 OHCI Host Controller

The Synopsys DesignWare USB 1.1 Host Controller (OHCI) Synthesizable IP is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB OHCI Host Controller function. Features include the following:

- Silicon proven
- USB 1.1 compliant
- AHB interface
- Compatible with Open HCI 1.0 specification
- Verilog source code
- Supports low-speed and full-speed devices
- Configurable root hub supporting up to 15 downstream ports
- Configuration data stored in Port Configurable Block
- Single 48-MHz input clock
- Simple application interface facilitates bridging the host to other system bus such as PCI, and the integration of the controller with chipsets and microcontrollers
- Integrated DPLL
- Support for SMI interrupts
- Approximately 25K gates with 2 ports



The dwcore_usb1_host datasheet is available at:

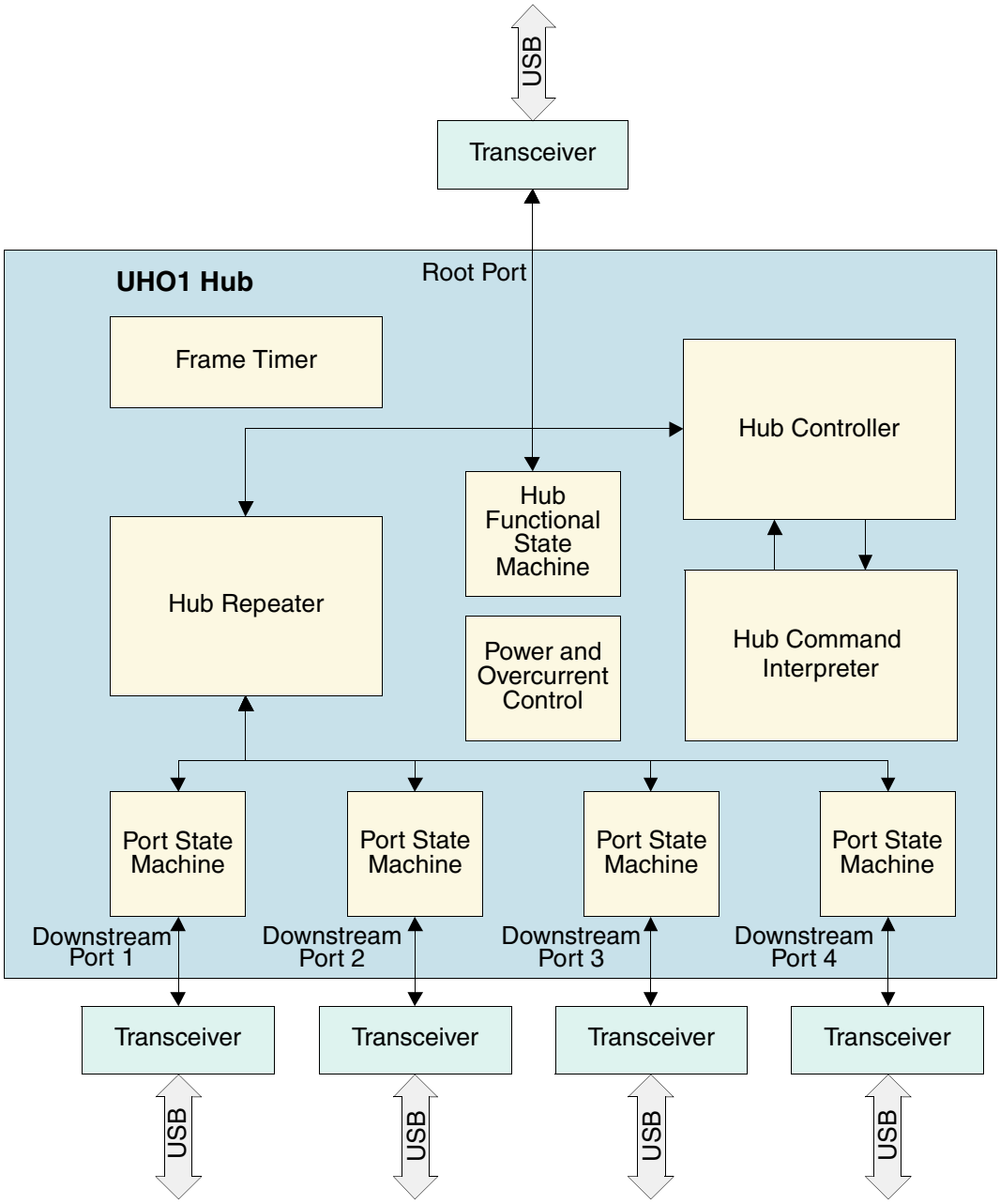
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb_1_1_ohci_host.pdf

dwc_usb_1_1_hub-native

Synthesizable USB 1.1 Hub Controller

The Synopsys DesignWare USB Hub (UH01) is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB Hub. The RapidScript utility enables designers to easily configure the device by setting the number of downstream ports. The Synopsys UH01 product consists of the Hub Repeater and the Hub Controller. The Hub Repeater is responsible for connectivity setup and tear-down and supports exception handling such as bus fault detection/recovery and connect/disconnect detection. The Hub Controller provides the mechanism for host to hub communication. Hub-specific status and control commands permit the host to configure a hub and to monitor and control its individual downstream ports. Other features include the following:

- Silicon proven
- USB 1.1 compliant
- Verilog source code
- Supports low-speed and full-speed devices on downstream ports
- Integrated DPLL for clock and data recovery
- Downstream device connect/ disconnect detection
- Supports suspend/ resume for power management
- Supports one interrupt endpoint in addition to endpoint 0
- Approximately 12K gates, for four ports



The dwcore_usb1_hub datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb_1_1_hub-native.pdf

dwc_usb_2_0_host_subsystem-pci-ahb

Synthesizable USB 2.0 Host Controller

The Synopsys DesignWare USB Host Controller (UHOST2) is a set of synthesizable building blocks that ASIC/FPGA designers use to implement a complete USB 2.0 host for 480-Mbps operation. The UHOST2 can be customized and optimized as a stand-alone host chip or as an integrated ASIC for applications such as game consoles, set-top boxes, PCs, PDAs, and telecommunications equipment. In addition, the design can be easily processed in most technologies and can be easily bridged to any industry-standard bus and includes both the PCI and ARM AHB interfaces. The application interface screens USB host controller design complexities, making it easy to integrate the UHOST2 device to customer target applications. Other features include the following:

General

- Design methodology supports full scan for testability
- All clock synchronization is handled within the controller
- coreConsultant utility provided for design configuration
- Descriptor and data prefetching (configuration option)
- No bidirectional or three-state buses
- No level-sensitive latches

Software

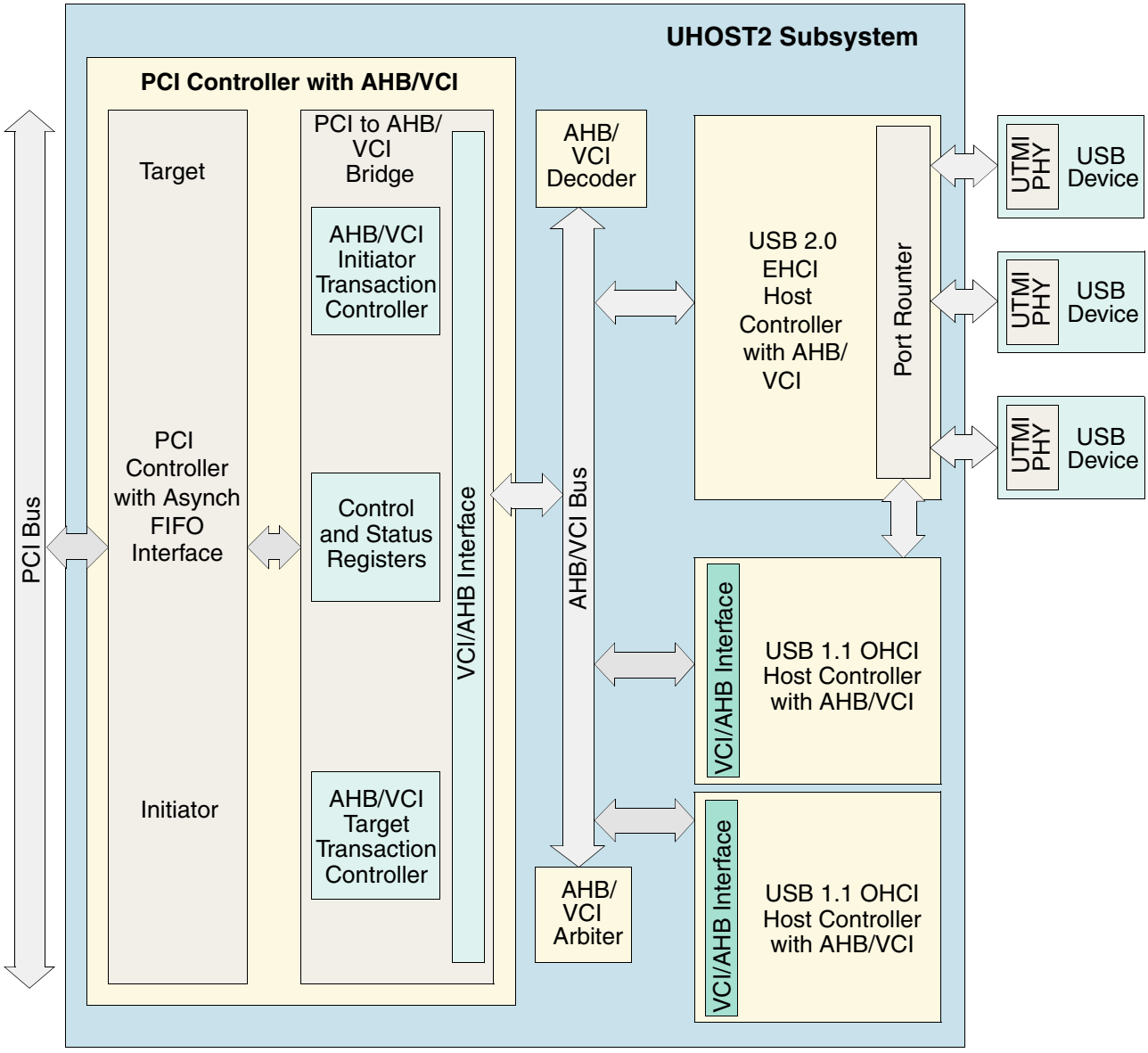
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

Power Optimization

- ULPI Reduced Power mode with ULPI wrapper operates at 60 MHz, with the remainder of the Root Hub operating at 30 MHz.

Application

- AHB interface to the application
- Complies with the AMBA Specification, Revision 2.0
- Bus Interface Unit (BIU) handles retry, error and split transactions on the AHB
- As an AHB Master supports 8-, or 32-bit data transfers on the AHB
- Supports 32-bit addressing on the AHB
- USB 2.0 Supported Features
- Complies with the USB 2.0 Specification
- Supports ping and split transactions
- UTMI+ or ULPI interface to the PHY
- UTMI PHY interface clock supports 30-MHz operation for a 16-bit interface or 60-MHz operation for an 8-bit interface
- ULPI PHY interface clock supports 60-MHz operation for both 8- and 4-bit interfaces



The dwcore_usb2_host datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb_2_0_host_subsystem-pci-ahb.pdf

dwc_usb_2_0_hs_otg_subsystem-ahb

Synthesizable Hi-Speed USB On-The-Go (OTG) Controller Subsystem

The DesignWare Hi-Speed USB On-The-Go (HS OTG) Controller Subsystem operates as either a Hi-Speed USB compliant peripheral, host, or OTG Dual-Role Device (DRD). This core has earned Hi-Speed USB OTG certification with the Synopsys USB OTG PHY in three semiconductor processes. Features include the following:

General Features

- Supports different clocks for AHB and the PHY interfaces for ease of integration
- Uses the coreConsultant utility to configure the core to user requirements
- Supports Slave, External DMA Controller Interface, or Internal DMA modes
- Includes USB power management features
- Includes power-saving features (clock gating, two power rails for advanced power management)
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs and flexible, efficient use of RAM
- Uses single-port RAM instead of dual-port RAM for smaller area and lower power
- Provides support to change an endpoint's FIFO memory size during transfers
- Supports endpoint FIFO sizes that are not powers of 2, to allow the use of contiguous memory locations
- Shares the hardware registers in the Host and Device modes to reduce gate count
- Supports the Keep-Alive in Low-Speed mode and SOFs in High/ Full-Speed modes
- Power-optimized design
- Optional support for Transmit and Receive thresholding in DMA mode when dedicated Tx FIFO is selected in Device mode. Thresholding and threshold length selectable through global registers. For supporting thresholding, the AHB must be run at 60 MHz or higher.
- NoteDedicated FIFO operation refers to the core configuration in which each Device mode IN endpoint has individual transmit FIFOs.
- Shared FIFO operation refers to the core configuration in which all non-periodic IN endpoints share a common TX FIFO and periodic IN endpoints have separate individual FIFOs.

USB 2.0 Supported Features

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports the UTMI+ Level 3 interface (Revision 1.0, February 25th, 2004). 8-, 16-, and
- 8/16-bit data buses are supported.
- Supports ULPI interface (Revision 1.1rc, September 1st, 2004) - 8-bit SDR, 4-bit DDR, 6-pin Serial, 3-pin Serial and Carkit
- The UTMI+ L3 and ULPI can both exist and be selected by software, or only the required interface can be specified during coreConsultant configuration.
- Supports Session Request Protocol (SRP)
- Supports Host Negotiation Protocol (HNP)
- I2C interface (for support of Mini USB Analog Carkit Interface Specification, CEA-936, Revision 2, not intended for use with other devices)
- Supports up to 16 bidirectional endpoints, including control endpoint 0
- Supports up to 16 host channels. In Host mode, when the number of device endpoints to be supported is more than the number of host channels, software can reprogram the channels to support up to 127 devices, each having 32 endpoints (IN + OUT), for a maximum of 4, 064 endpoints.
- Supports a generic root hub
- Includes automatic ping capabilities

Software Features

- To increase flexibility and reduce gate count, certain functions are implemented in software:
- Software assists hardware for Device mode non-periodic IN sequencing (applicable only in Shared FIFO operation).
- Software handles USB commands (SETUP transactions are detected and their command payloads are forwarded to the application for decoding).
- Software handles USB errors.

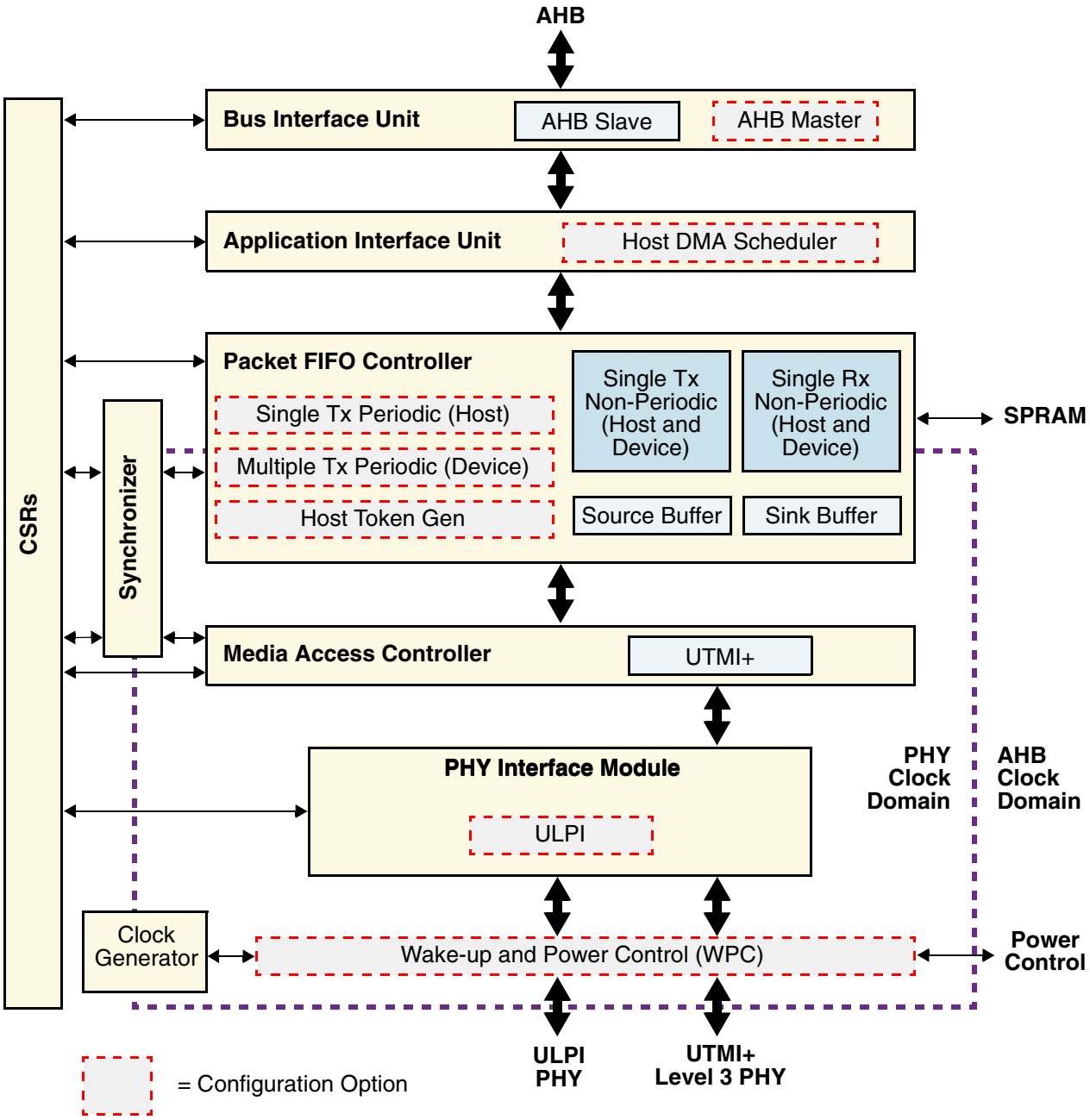
Power Optimization Features

- PHY clock gating support during USB Suspend mode and Session-Off mode
- AHB clock gating support during USB Suspend mode and Session-Off mode
- Partial power-off during USB Suspend mode and Session-Off mode
- Hierarchy to support multiple power rails
- Input signals to powered-off blocks driven to safe 0
- Data FIFO RAM chip-select deasserted when not active
- Data FIFO RAM clock-gating support

Application Features

- Interfaces for the application via the AHB:
- AHB Slave interface for accessing Control and Status Registers (CSRs), the Data FIFO, and queues
- Optional AHB Master interface for Data FIFO access when Internal DMA is enabled
- Supports AHB clock frequencies up to 180 MHz with suitable technology (for example, a standard 0.13 micron technology)
- Supports only 32-bit data on the AHB
- Supports Little or Big Endian mode (selectable by pin)
- Supports all AHB burst types in AHB Slave interface
- Supports Split, Retry, and Error AHB responses on the AHB Master interface; these are not generated on the AHB Slave interface
- Software-selectable AHB burst type on AHB Master interface
- If INCR4 is chosen, core only uses INCR4.
- If INCR8 is chosen, core normally uses INCR8, but at the beginning and at the end of a transfer, it can use INCR4, depending on the size of the transfer.
- If INCR16 is chosen, core normally uses INCR16, but at the beginning and at the end of a transfer, it can use INCR4/INCR8, depending on the size of the transfer.
- Handles the fixed burst address alignment. For example, INCR16 is used only when lower addresses [5:0] are all 0.
- Generates AHB Busy cycles on the AHB Master interface
- Takes care of the 1KB boundary breakup.
- Includes optional interface to an external DMA controller; data is transferred through the AHB Slave interface.
- Optional support for a dedicated transmit FIFO for each of the device IN endpoints in Slave and DMA modes. Each FIFO can hold multiple packets.

DWC Hi-Speed USB OTG Controller



The dwcore_usb2_hsotg datasheet is available at:

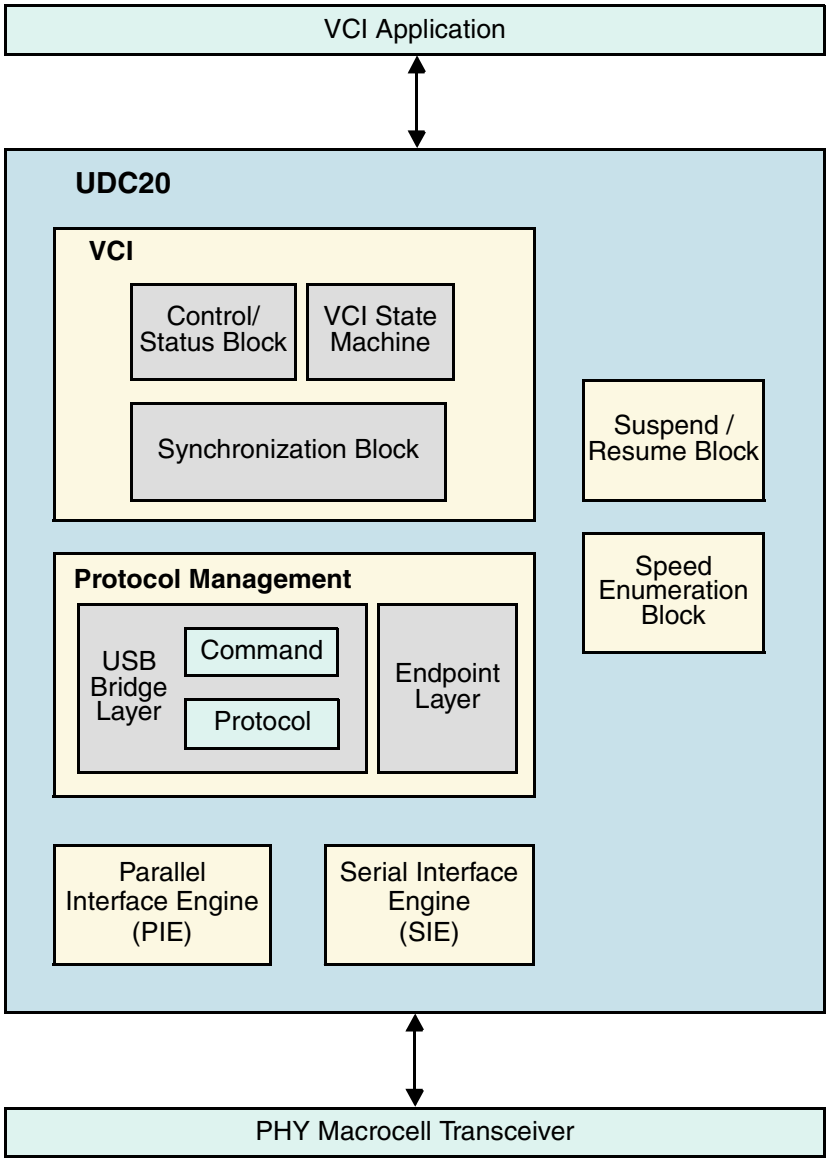
http://www.synopsys.com/products/designware/docs/ds/c/dwc_usb_2_0_hs_otg_subsystem-ahb.html

dwc_usb_2_0_device

Synthesizable USB 2.0 Device Controller

The USB 2.0 Device Controller (UDC20) features industry-standard interfaces that easily integrate the USB 2.0 transceiver and application logic. The RapidScript utility builds the core and test environment in source code for the targeted application. Other features include the following:

- Complies with USB 2.0 and USB 1.1 protocols
- Integrates the UDC20/UDCVCI USB device controllers from Synopsys
- Supports high-speed (480 MHz), full-speed (12 MHz) and low-speed (1.5 MHz) operations for UDC20, and supports full-speed and low-speed operations for UDCVCI
- Supports AHB clock (hclk_i) frequencies of 12–133 MHz for UDC-VCI. For UDC20, the range is 16 to 133 MHz.
- Supports up to 16 IN and 16 OUT physical endpoints, which can be tied to different interfaces and configurations to achieve logical endpoints
- Permits user control through memory-mapped control and status registers (CSRs)
- Enables user-configurable endpoint information
- Supports both DMA option and Slave-Only modes
- Supports true scatter-gather DMA implementation
- Supports descriptor-based memory structures in application memory when in DMA mode
- Ideally suited for portable handheld applications requiring optimal memory usage
- Supports adaptive buffering for efficient IN endpoint buffer management
- Completely synchronous design (clock boundary is in the subsystem)
- Supports power management
- In full and high speed operation, UDC-AHB subsystem is compatible with UTMI+ level 3 PHY
- Supports the following UTMI data bus interfaces:
  - Unidirectional 8-bit interface
  - Unidirectional 16-bit interface
  - Bidirectional 8-bit interface
  - Bidirectional 16-bit interface
- ULPI functions defined in the ULPI specification (version 1.0rc) are supported with the following exceptions:
- ULPI in Low Speed mode is not supported
- 60 MHz-only clock speed
- UTMI data width is normally 8 bits input/output
- DDR nibble operation is supported
- OTG, Carkit features are not supported



The dwcore_usb2_device datasheet is available at:

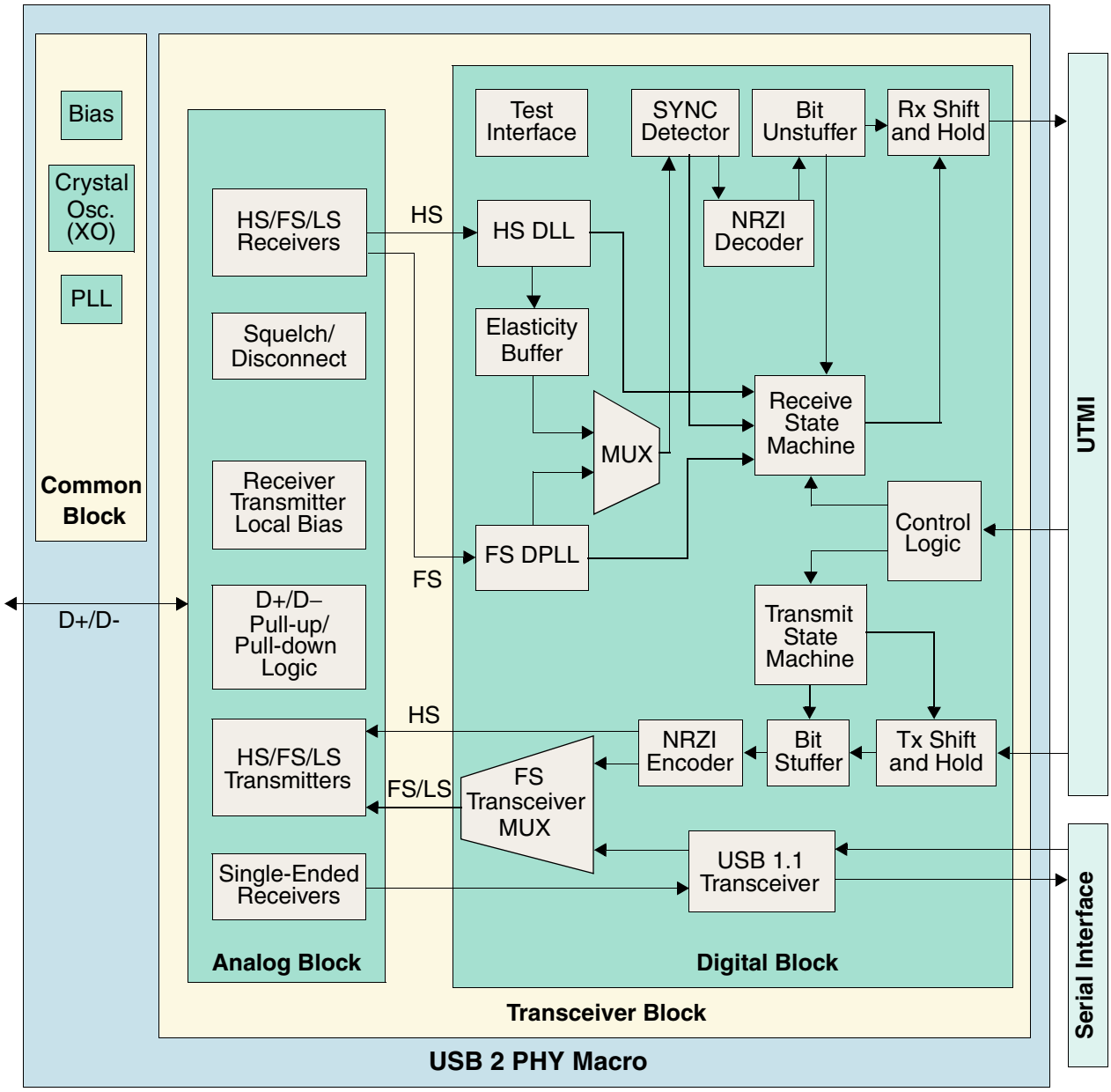
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb_2_0_device.pdf

dwc_usb2_phy

USB 2.0 Transceiver Macrocell Interface PHY

The USB 2 PHY includes all the required logical, geometric and physical design files to implement USB 2.0 capability in a System-on-Chip (SOC) design and fabricate the design in the designated foundry. The initial foundry process for the USB 2 PHY is the 0.18-micron CMOS digital logic process. Alternatively, design services are available for porting the USB 2 PHY to other semiconductor processes. The USB 2 PHY integrates high-speed, mixed-signal, custom CMOS circuitry compliant with the UTMI Specification (version 1.05), supports the USB 2.0 480-Mbps protocol and data rate, and is backward compatible to the USB 1.1 legacy protocol at 1.5-Mbps and 12-Mbps. Other features include the following:

- Complete mixed-signal physical layer (PHY) for single-chip USB 2.0 applications
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification compliant
- 8-bit interface at 60-MHz operation and 16-bit interface at 30-MHz operation chip
- Compatible with the Synopsys USB 2.0 Device and Host components
- USB 2.0 Device automatic switching between full- and high-speed modes
- Host Device automatic switching between full-, high- and low-speed modes
- Designed for minimal power dissipation for low-power and bus-powered devices
- Low-power design enables host enumeration of an unpowered device
- Sea-wall and decoupling structures reduce on-chip noise
- Suspend, Resume and Remote Wake-up mode support
- USB 2.0 test mode support
- Additional built-in analog testability features
- USB Implementers Forum certified



The dwcore_usb2_phy datasheet is available at:

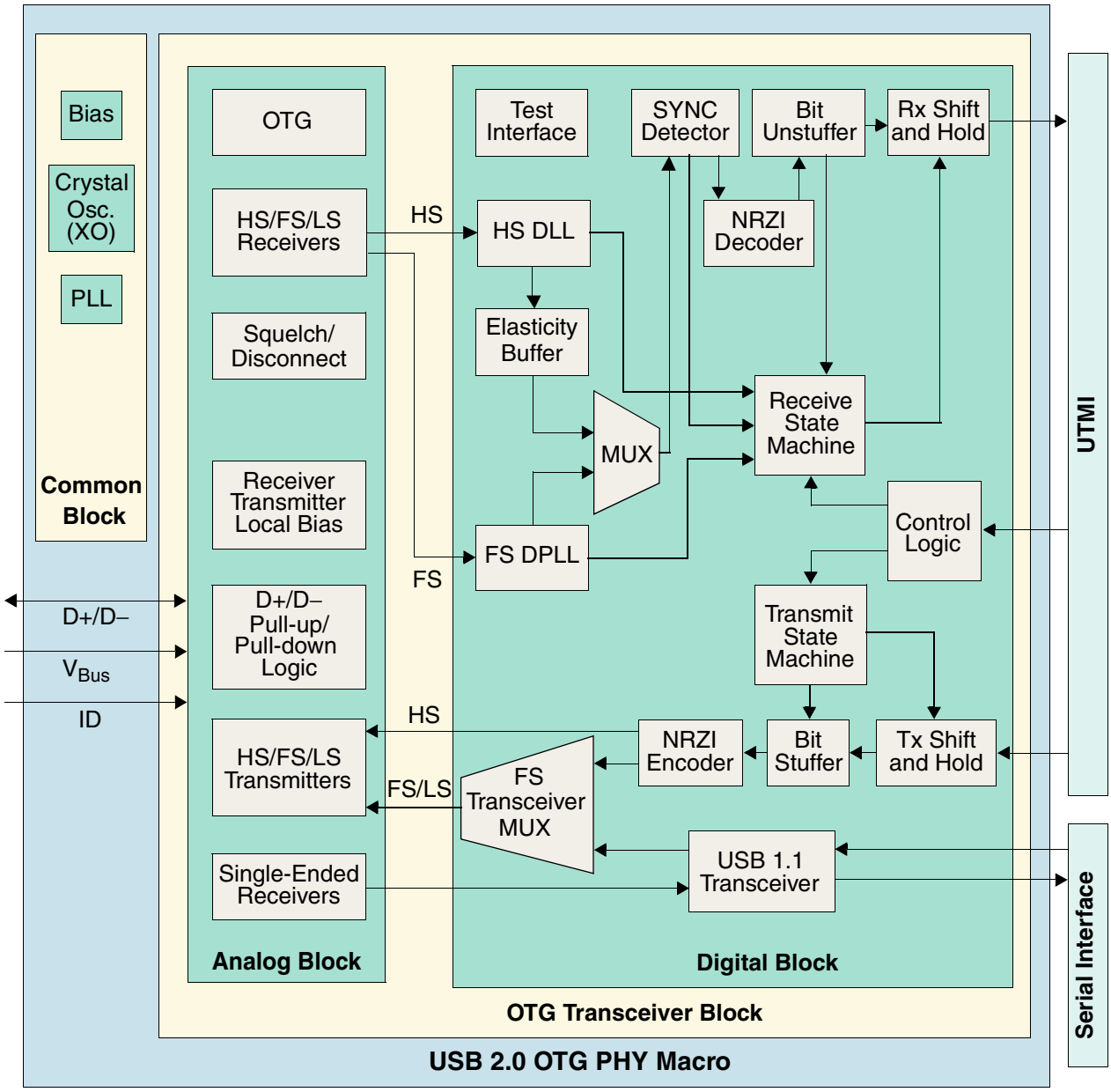
http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb2_phy.pdf

dwc_usb2_hsotg_phy

USB 2.0 Hi-Speed OTG PHY

The Synopsys DesignWare Hi-Speed USB 2.0 On-The-Go (HS OTG) PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip, USB 2.0 integration in OTG applications. The USB 2.0 OTG PHY includes all the required logical, geometric, and physical design files to implement USB 2.0 Hi-Speed OTG capability in a system-on-chip (SoC) design and to manufacture it in the designated foundry. The USB 2.0 OTG PHY is available in 90-nanometer (nm), 130-nm, and 180-nm CMOS digital logic processes.

- Complete mixed-signal physical layer (PHY) for single-chip USB 2.0 OTG applications
- USB 2.0 Transceiver Macrocell Interface (UTMI+ Level 3) specification
- 8-bit interface at 60-MHz operation and 16-bit interface at 30-MHz operation
- Hi-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) operation is compliant to the USB OTG Supplement
- Supports all OTG features, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Designed for rapid integration with Synopsys's HS USB 2.0 OTG controller
- Designed for minimal power dissipation for low-power and bus-powered devices
- Verified in 90-nm, 130-nm, and 180-nm silicon
- Based on Synopsys's USB Implementers Forum certified HS USB 2.0 PHY architecture



The dwc_usb2_hsotg_phy datasheet is available at:

http://www.synopsys.com/cgi-bin/dwcores/pdfr1.cgi?file=dwc_usb2_hsotg_phy.pdf

dwc_wiusb_device_controller

Wireless USB Device Controller

Synopsys DesignWare Wireless USB (WiUSB) Device Controller IP, based on the Wireless USB specification from the USB-IF, provides designers with a high-performance WiUSB IP core for SoC integration. The WiUSB Device Controller enables a wide range of portable electronics or PC peripherals the ability to connect without cables and delivers a conservative timing for implementation into a broad range of ASIC and FPGA technologies.

Synopsys designed its DesignWare WiUSB IP core using low-power flows and a low-power architecture, with clock gating and two power rails, to minimize area and power consumption. An extensive verification process, which includes simulation and hardware interoperability testing, enables Synopsys to deliver a high-quality IP core, that lowers overall integration risk and shortens time to results. As a technical contributor to the Certified Wireless USB specification and a member of the WiMedia Alliance standards committee, Synopsys focuses on delivering the highest quality interoperable Wireless USB IP for our customers.

WiMedia Ultra-Wideband (UWB) MAC

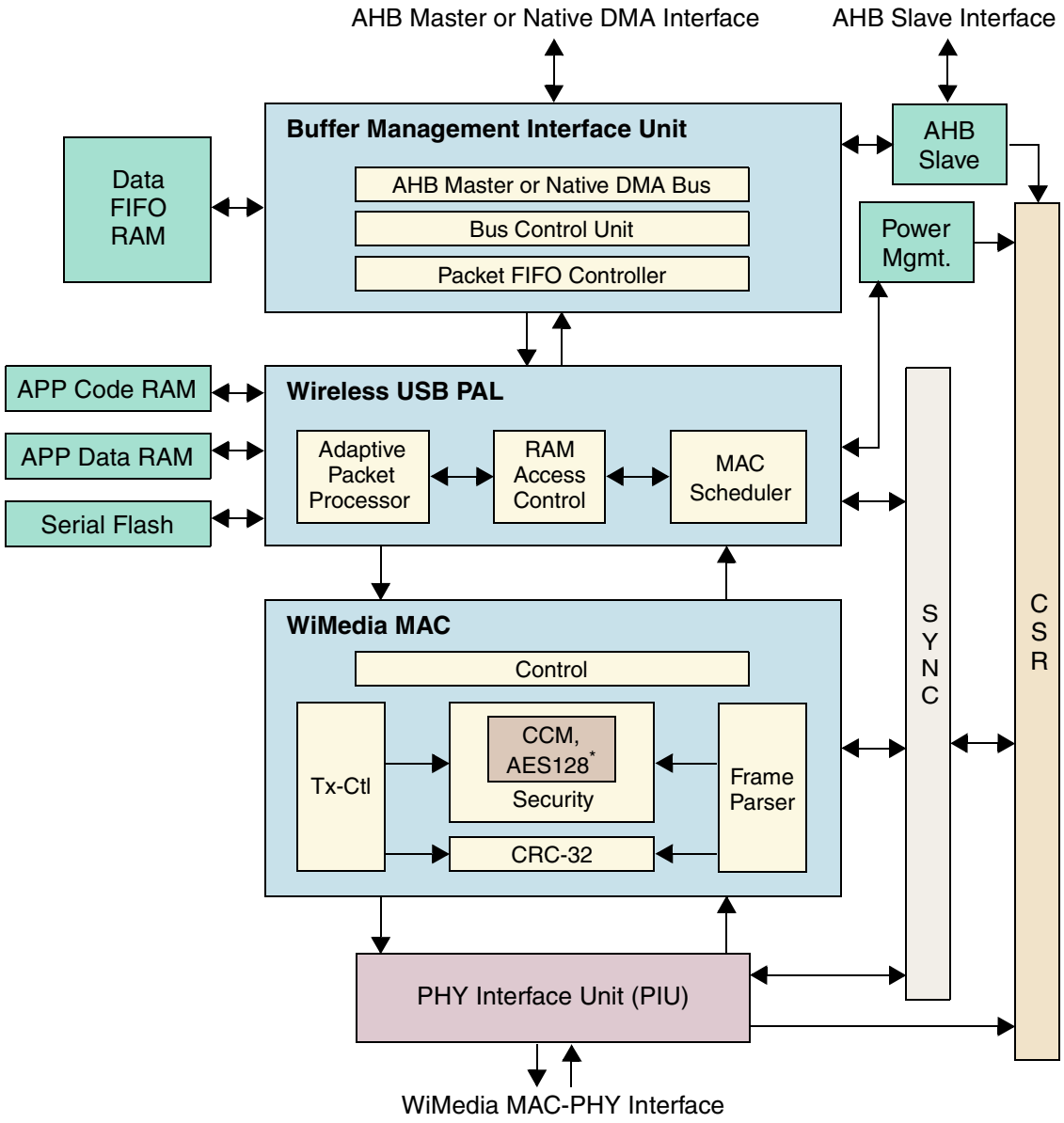
- Supports WiMedia Ultra-Wideband (UWB) Common Radio Platform
- Modular design for power savings in all layers
- Support for MIC generation with UWB AES-128-bit encryption block
- Standard MAC PHY interface for connection to external discrete PHYs or internal integrated PHYs
- Asynchronous clock domains support different PHY frequencies. This allows the use of a separate PHY clock and MAC clocks

Buffer Management Unit (BMU)

- Flexible interface can be configured for high performance and throughput
- AHB Master or Native interface with DMA engine reduces microprocessor loading and maximizes performance
- FIFO sizes are adjustable to tune for performance or die area to focus on throughput or cost

Wireless USB Protocol Adaptation Layer (PAL)

- Protocol Adaptation Layer (PAL) based on Wireless USB from the USB-IF
- Adaptive Packet Processor (APP) allows for post-silicon upgrades to firmware and protocol processing, and additional features (sold separately)
- Device controller includes features for adding CWUSB to a PC peripheral, such as a printer or a portable CE device, such as a camera



The DesignWare dwc_wiusb_device_controller datasheet is available at:

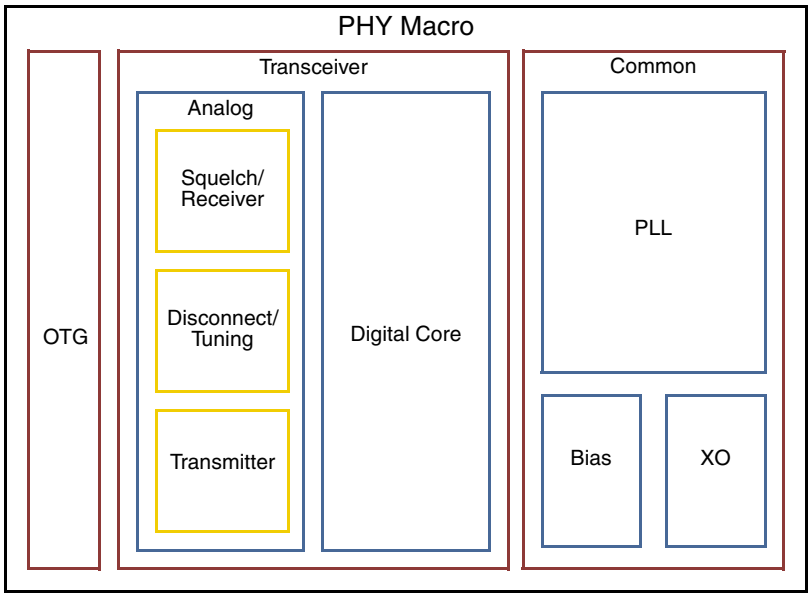
http://www.synopsys.com/products/designware/wiusb_solutions.html

dwc_usb2_nanophy

USB 2.0 nanoPHY

The USB 2.0 nanoPHY provides designers with a complete Physical Layer (PHY) IP solution, designed for low-power mobile and consumer applications such as next-generation handheld game machines, feature-rich smart phones, digital cameras, and portable audio/video players. The DesignWare USB 2.0 nanoPHY IP delivers approximately half the power and die area compared to other solutions, for longer battery life and lower silicon cost. Designed for high yield, the DesignWare USB 2.0 nanoPHY implements architectural features that make it less sensitive to variations in foundry process, device models, package and board parasitics. Other features include the following:

- Complete mixed-signal physical layer for single-chip USB 2.0 OTG and non-OTG applications
- Low power: ~100 mW (during HS packet transmission)
- Small area: ~ 0.6 mm^2
- High yield: Architecture designed to improve key operating margins by having less sensitivity to variations due to foundry process, chip and board parasitics, and process device model variations
- Designed for the latest 65-, 90-, and 130-nm low power (LP) CMOS processes
- Low pin count
- USB 2.0 Transceiver Macrocell Interface (UTMI+ Level 3) specification
- 8-bit interface at 60-MHz operation and 16-bit interface at 30-MHz operation
- Hi-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation is compliant with the USB 2.0 OTG Supplement
- Supports all OTG features, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Designed for rapid integration with the Synopsys USB 2.0 Hi-Speed OTG controller
- On-chip PLL reduces clock noise and eliminates external clock generator requirement
- Built-in VBUS pulsing and discharge SRP circuitry
- Built-in VBUS threshold comparators
- Supports off-chip charge pump regulator to generate 5-V VBUS signals
- Designed for minimal power dissipation for low-power and bus-powered devices
- Supports Suspend, Resume, and Remote Wakeup modes
- Supports USB 2.0 test modes



The dwc_usb2_nanophy datasheet is available at:

http://www.synopsys.com/products/designware/docs/ds/c/dwc_usb2_nanophy.pdf

dwc_xaui_phy
XAUI PHY IP

The DesignWare XAUI PHY IP is designed for use in any networking or high-end, computing SoC solutions. Designed for the latest high-speed backplanes, the DesignWare XAUI PHY supports the 10-gigabit Ethernet standards that are commonly used in high-speed communications applications. Based on Synopsys's silicon-proven and award-winning high-speed SERDES technology, the XAUI PHY provides a cost-effective and extremely low-power solution designed to meet the needs of today's XAUI designs.

Designed for advanced manufacturing processes, the XAUI PHY is targeted to popular low-power and high-performance CMOS digital logic processes. The XAUI PHY integrates high-speed mixed-signal custom CMOS circuitry compliant with the XAUI IEEE base specification 802.3ae. While extremely low in power consumption and area requirements, the DesignWare XAUI PHY substantially exceeds the electrical specifications in key performance areas such as jitter and receiver sensitivity.

To handle increasing communication system speeds, the XAUI standard was designed to take a 10-Gbps serial stream and divide it into four 2.5-Gbps serial streams that run over copper traces and chip-to-chip connections using 8b10b coding at 3.125 Gbaud. By taking advantage of copper links, higher performance communications applications can be cost effectively deployed.

Features

- Supports 10GBASE-CX4
- Transmits 3.125 Gbps differential NRZ serial stream
- Receives 3.125 Gbps differential NRZ serial stream
- Supports asynchronous operation
- Supports both 10-bit and 20-bit parallel ASIC interfaces
- Supports popular data rates: 3.125 Gbps, 3.0 Gbps, 2.5 Gbps, 1.5 Gbps, and 1.25 Gbps
- Provides on-die scope and diagnostics for fast system verification
- Small, cost-effective die size
- Supports popular 130-nm, 90-nm, and 65-nm common platform processes
- Supports 4x and 8x lane widths
- Supports many reference clock frequencies: 25 MHz–156.25 MHz, including popular 125-MHz and 156.25-MHz clocks
- Interoperable with the Synopsys DesignWare XGXS-PCS IP
- Provides flexible Tx pre-emphasis and Rx equalization settings to support a variety of lossy channels

Performance

- Low-jitter PLL technology with excellent supply isolation
- Low-offset, high-sensitivity receiver with high resolution CDR
- Robust PHY architecture, tolerates wide PVT variations
- Short training sequences and fast transitions between power states enable highly efficient operation
- ± 10% supply variation
- Excellent performance margin and receive sensitivity
- Very low power design—down to half the power compared to conventional PHYs

The DesignWare dwc_xaui_phy datasheet is available at:

http://www.synopsys.com/products/designware/docs/ds/c/dwc_xaui_phy.pdf

5 DesignWare Star IP

Design engineers who use the DesignWare Library have the ability to evaluate and design easily at their desktop using the following high-performance, high-value IP cores from leading Star IP providers. All DesignWare Star IP cores are packaged with the Synopsys coreConsultant tool which guides the user through the installation, configuration, verification and implementation.

Component Name	Component Description	Component Type[a]
DW_IBM460-S, DW_IBM405-S	PowerPC 32-Bit Microprocessor Cores from IBM (page 177)	Synthesizable RTL[a] Simulation Models
DW_CoolFlux	CoolFlux 24-bit DSP Core from NXP (page 179)	Synthesizable RTL[a] Simulation Model
DWC_n2p	Nios II Processor Core (page 182)	Synthesizable RTL[a]

a. Simulation models of these cores are available to all active DesignWare Library licensees and accessed through the Synopsys website. Synthesizable RTL (implementation views) of these cores are available from Synopsys and/or their respective IP providers.

DW_IBM460-S, DW_IBM405-S

IBM PowerPC 460 and 405 CPU Cores

Overview

The IBM PowerPC® 460/405 cores are portable and synthesizable implementations of the PowerPC 460 and 405 32-bit RISC CPU cores. The Power PC 405-S core employs the scalable and flexible Power ISA™ 2.03, and the PowerPC 460-S core employs the powerful Book-E Enhanced PowerPC Architecture™. Both cores are optimized for embedded applications.

Highlights

- Fully synthesizable to provide portability to any foundry or process technology (460-S and 405-S)
- Customizable to enable you to target various performance, power, area or other implementation goals
- AMBA AHB interface supports connection to industry-standard peripherals (for example, DesignWare AMBA components) for ease of SoC integration
- Integrated functions in the PowerPC 460/405 CPUs include instruction and data caches, memory management unit (MMU), timers, and a JTAG debug port.
- A comprehensive portfolio of the PowerPC family support tools is available through the IBM Business Partners network. Offerings include operating systems, compilers, debuggers, simulators and emulators, and design services

DesignWare PowerPC IBM 460/405 Benefits

- Complete, silicon-tested processor subsystem
- Ready to use: just add your choice of memories and peripherals (460-S and 405-S). A set of CoreConnect PLB4 peripherals are available at no extra charge to PowerPC 460/405 licensees.
- Industry standard DesignWare IP delivery package
- Industry-leading technical support team
- Implementation View delivered as Verilog source
- AMBA AHB for easy connection to peripherals
- Tested against latest versions of Synopsys tools and other third-party simulation tools

Table 1: PowerPC 460/405 CPU Core Sample Specifications

Technology	90nm (Worst-case conditions)
Temperature	125° C
Voltage	1.08 v
Frequency	400 MHz (460-S) 400 MHz (405-S)
Die Size	8.31 mm^2 (460-S) 1.69 mm^2 (405-S)
Power Dissipation	5.27 mw/MHz, WC Process (460-S), 0.96 mw/MHz, WC Process (405-S)

See the following web page for additional information:

http://www.synopsys.com/IP/DesignWare/StarIP/Pages/IBMPowerPC.aspx

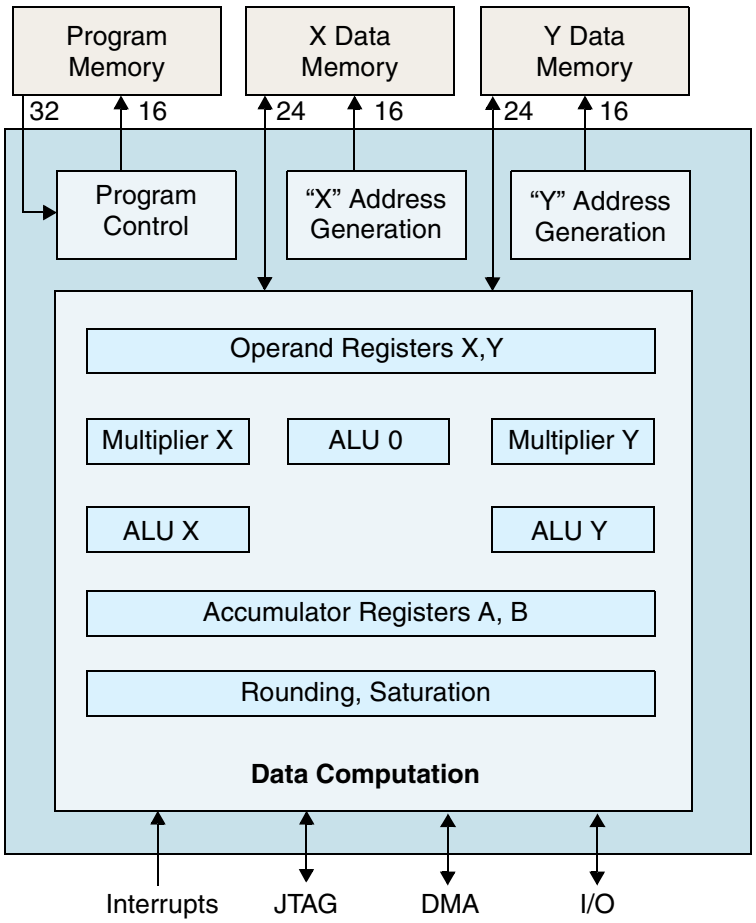
DW_CoolFlux

CoolFlux 24-bit DSP Core from NXP

The NXP CoolFlux DSP is a synthesizable 24-bit DSP Core for ultra-low power applications like portable audio encoding/decoding, sound enhancement, and noise suppression. The core targets specific applications such as headsets, hearing instruments, and portable audio players. The NXP CoolFlux DSP is designed with a highly efficient ILP optimizing C compiler. The compiler can exploit all the parallelism in the core and generates very efficient code, both from a cycle and code density perspective.

Other features include the following:

- Ultra low power consumption:
  - < 0.1mW/MHz @ 1.2V (0.13µ CMOS)
  - < 0.2m W/MHz @ 1.8V (0.18µ CMOS)
- Highly optimizing C-compiler
- Minimal core size (43K gates, excluding debug interface 4.5k gates)
- Small memory footprint
- Performance (worst case commercial conditions):
  - 175 MHz (0.13µ CMOS)
  - 135 MHz (0.18µ CMOS): >1000 MOPs
- Extensive software library for audio decoding and advanced sound enhancement algorithms
- Dual Harvard architecture
- Full 24-bit data paths
- Two 24 x 24 bit signed multipliers
- Three ALUs
- Four 56-bit accumulators
- Extensive addressing modes with modulo protection, bit reversal
- Saturation and rounding units
- RISC instruction set suitable for control, as well as DSP
- Highly efficient stack support
- Zero overhead loops (nested up to 4 levels)
- 64 Kwords address space each for P, X, Y, IO
- DMA ports for program and data memories
- Three maskable low latency interrupts
- Extensive power management support (stop / restart instructions)
- JTAG-based (Joint Test Action Group IEEE 1149.1 std. test interface) debug port



Also see the following web page for additional information:

http://www.synopsys.com/IP/DesignWare/StarIP/Pages/CoolFlux.aspx

Star IP

DWC_n2p

Nios II Processor Core

The Designware Nios® II Processor from Synopsys, also referred to as DWC_n2p in this document, is an ASIC implementation of Altera's popular Nios® II configurable general-purpose 32-bit RISC processor.

DWC_n2p is a single module that contains an embedded Nios II Processor and additional logic for system level debug through a JTAG interface. Users can specify configuration parameters to optimize the DWC_n2p hardware to match their system requirements.

Features

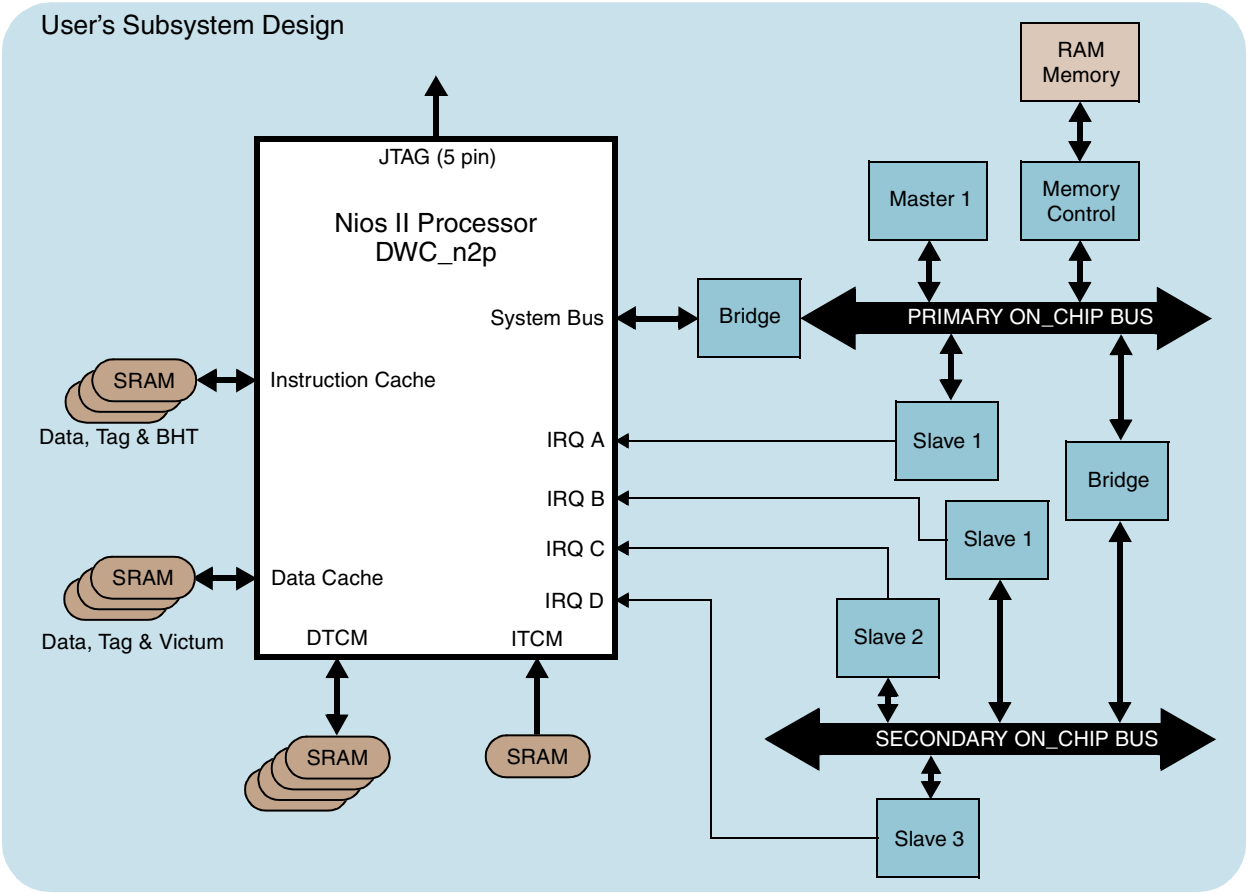
- Full 32-bit Instruction Set
- Thirty-two 32-bit general purpose registers
- Four external interrupt sources
- Combined instruction and data system port (Von Neumann Architecture)
- Support for a single optional Instruction Tightly Coupled Memory
- Support for up to 4 optional Data Tightly Coupled Memories
- Exported interface for Cache / TCM memories
- Optional exported interface for data cache memories (data cache can be omitted)
- Dynamic branch prediction minimizes taken branch penalty
- 6-stage pipelines to achieve maximum DMIPS/MHz
- 500 DMIPS Performance
- Single instruction barrel shifter
- Single instruction 32 x 32 multiply producing a 32-bit result
- Single instruction 32 x 32 divide producing a 32-bit result
- Embedded hardware-assisted On-Chip Debug (OCD) module enabling start, stop and step
- 5 pin JTAG interface with embedded tap controller for OCD debug
- Embedded JTAG UART for stdio comm.
- Embedded timer module for Nios II software backward compatibility
- Full compatibility with the Nios II Integrated Development Environment
- Compatible with software environment based on the GNU C/C++ tool chain and Eclipse

Unsupported NIOS II Features

- No Separate Instruction and Data Master ports (Harvard architecture)
- No Avalon burst protocol (Nios II Processor transfers are issued as single)
- No floating point instructions for single-precision floating point operations
- No instructions for computing 64-bit and 128-bit products
- Data Master system memory port is not removable (needed for OCD)
- No level 2 & level 3 debug support (no support for HW breakpoint and trace)

Key Configurability Options

- Instruction Cache Size: 512 – 64K
- Instruction TCM Interfaces: 0 or 1
- Instruction TCM Size: 512 – 64K
- Allow Data Writes to ITCM: Yes/No
- Number of Data TCM: 0-4
- Data TCM Size: 512 – 64K
- Data Cache Size: 0 – 64K
- Cacheless Option to remove both Data Cache and DTCM
- External Interrupts: 0-4
- Configurable Priority Level per Interrupt



Nios II FPGA Base Configuration Options

Table 1 shows the Nios II FPGA base configuration options:

Table 1: Nios II FPGA Base Configuration Options

	Nios II / f Fast Processor	Nios II / s Standard Processor	Nios II / e Economy Processor
Pipeline	6 stage	5 stage	None
Hardware multiplier and barrel shifter	1 cycle	3 cycle	Emulated in software
Branch prediction	Dynamic	Static	None
Instruction cache	Configurable	Configurable	None
Data cache	Configurable	None	None
Custom instructions	Up to 256		

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